GENERAL DESCRIPTION

OB2268/9 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications in above 20W power level.

PWM switching frequency at normal operation is externally programmable and trimmed to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved.

VDD low startup current and low operating current contribute to a reliable power on startup design with OB2268/9. A large value resistor could thus be used in the startup circuit to minimize the standby power.

The internal slope compensation improves system large signal stability and reduces the possible sub-harmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense input removes the signal glitch due to snubber circuit diode reverse recovery. and greatly reduces the external component count and system cost in the design.

OB2268/9 offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), over temperature protection (OTP), VDD over voltage protection (OVP) and under voltage lockout (UVLO). The Gate-drive output is clamped to maximum 18V to protect the power MOSFET.

Excellent EMI performance is achieved with On-Bright proprietary frequency shuffling technique (OB2269 only) together with soft switching control at the totem pole gate drive output.

The tone energy at below 20KHZ is minimized in operation. Consequently, audio noise performance is greatly improved.

OB2268/9 is offered in SOP-8 and DIP-8 packages.

FEATURES

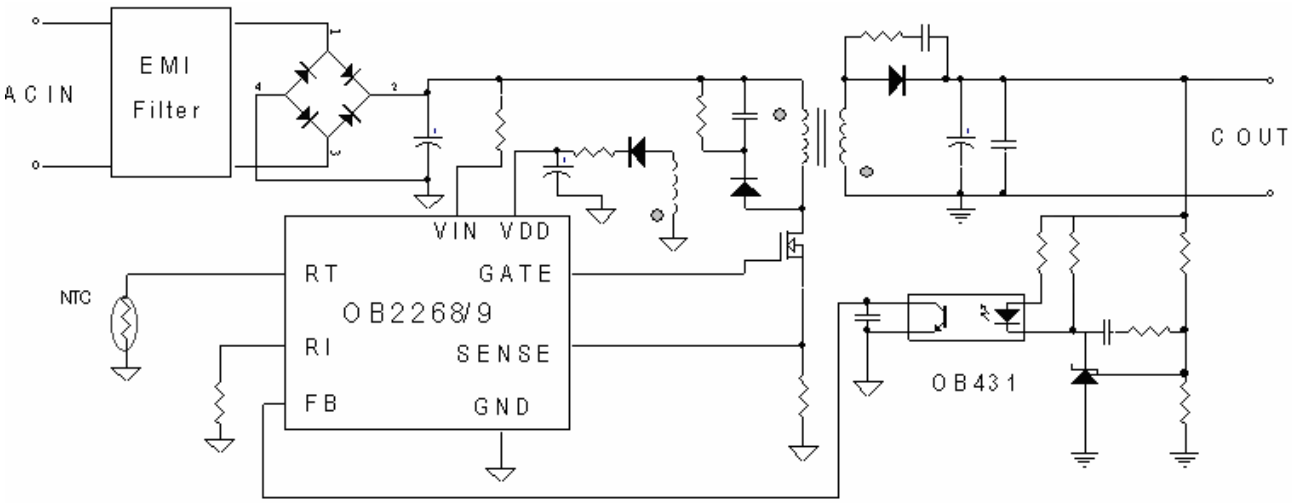
- Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design
- Audio Noise Free Operation
- External Programmable PWM Switching Frequency
- Internal Synchronized Slope Compensation
- Low VIN/VDD Startup Current(4uA) and Low Operating Current (2.3mA)
- Leading Edge Blanking on Current Sense Input
- Complete Protection Coverage With Auto Self-Recovery
  - External Programmable Over Temperature Protection (OTP)
  - With or Without On-chip VDD OVP for Output Over Voltage Protection.
  - Under Voltage Lockout with Hysteresis (UVLO)
  - Gate Output Maximum Voltage Clamp (18V)
  - Line Compensated Cycle-by-Cycle Over-current Threshold Setting For Constant Output Current Limiting Over Universal Input Voltage Range (OCP)
  - Over Load Protection. (OLP)
- On-Bright Proprietary Frequency Shuffling Technology for Improved EMI Performance (OB2269 only)

APPLICATIONS

Offline AC/DC flyback converter for

- Laptop Power Adaptor
- PC/TV/Set-Top Box Power Supplies
- Open-frame SMPS
- Battery Charger

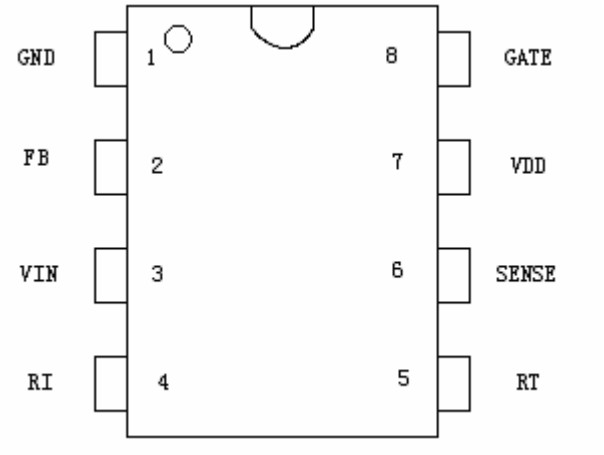
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The OB2268/9 is offered in DIP and SOP packages shown as below.



Ordering Information

Part Number	Description
OB2268AP	No Frequency Shuffling, DIP8, Pb-free
OB2268APV	No Frequency Shuffling, DIP8, Pb-free and no OVP
OB2269CP	With Frequency Shuffling, SOP8, Pb-free
OB2269CPV	With Frequency Shuffling, SOP8, Pb-free and no OVP

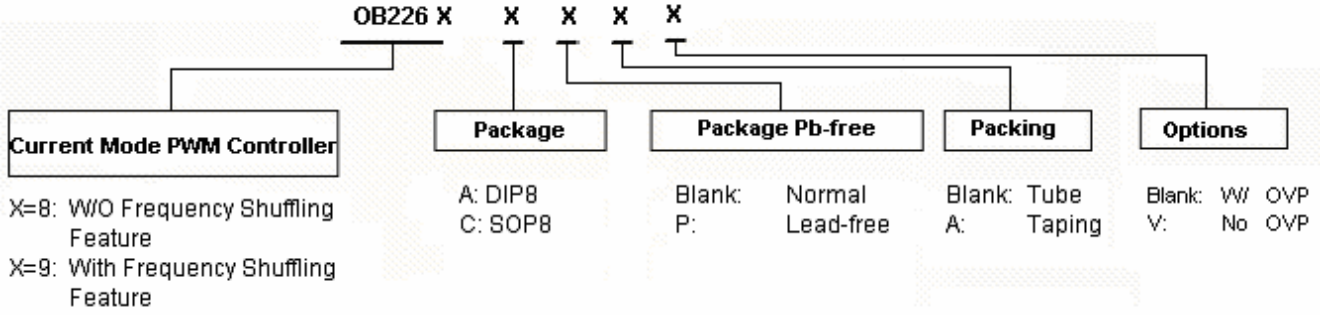
Package Dissipation Rating

Package	RθJA (°C/W)
DIP8	90
SOP8	150

Absolute Maximum Ratings

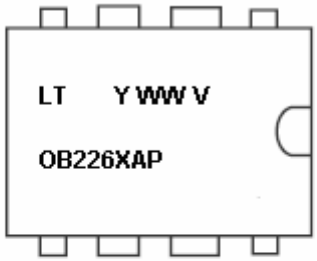
Parameter	Value
V_{DD} Input Voltage	36 V
VIN Input Voltage	36 V
V_{DD} Clamp Continuous Current	10 mA
V_{FB} Input Voltage	-0.3 to 7V
V_{SENSE} Input Voltage to Sense Pin	-0.3 to 7V
V_{RT} Input Voltage to RT Pin	-0.3 to 7V
V_{RI} Input Voltage to RI Pin	-0.3 to 7V
Min/Max Operating Junction Temperature T_J	-20 to 150 °C
Min/Max Storage Temperature T_{stg}	-55 to 150 °C

Note: Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.



Marking Information

DIP8



X: 8 - W/O Freq Shuffling
9 - With Freq Shuffling
A: DIP8 Package
P: Pb-free package (norm if blank)
Y: Year Code(0-9)
WW: Week Code (01-52)
V: W/O OVP(norm if blank)

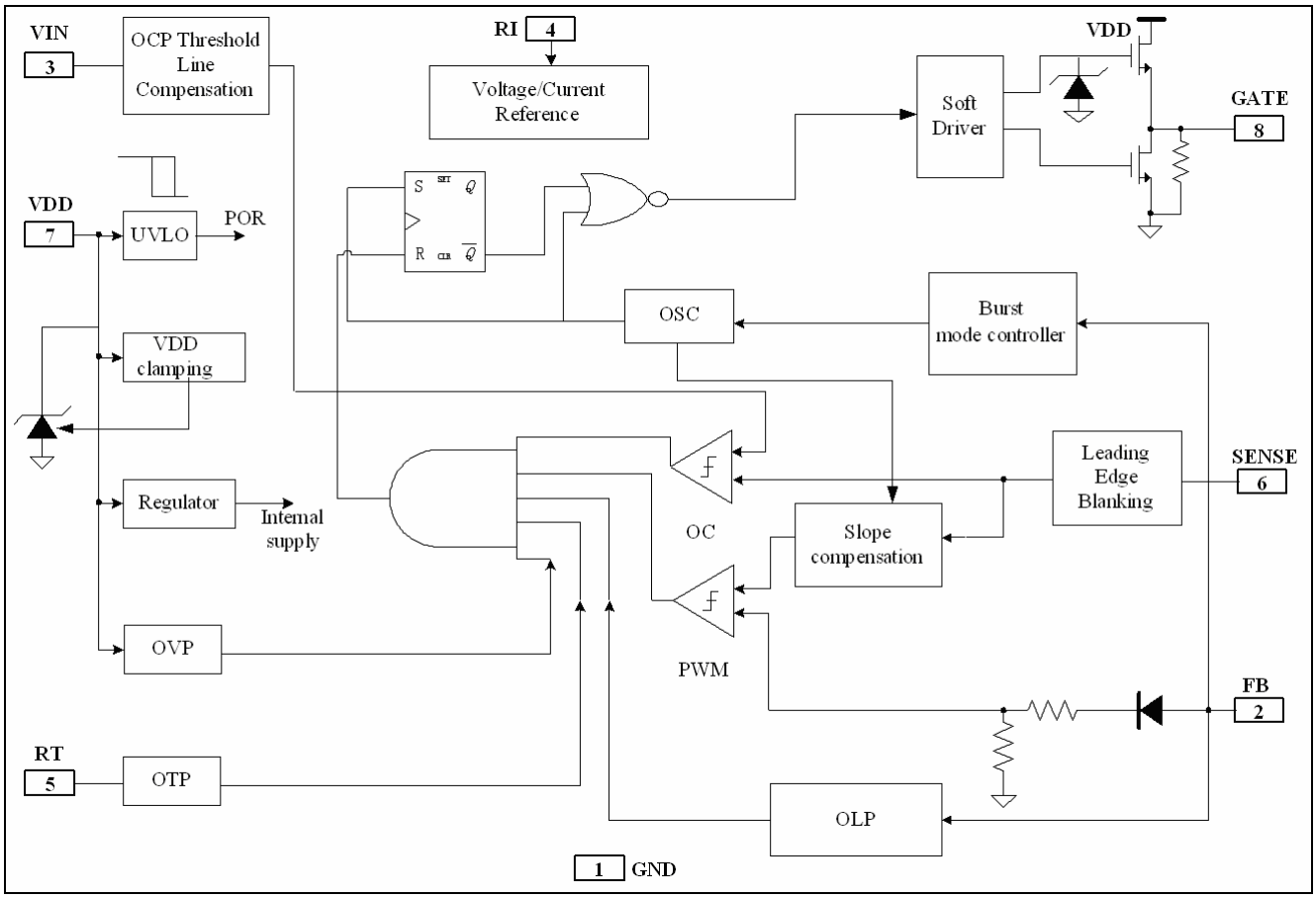
SOP8

X: 8 - W/O Freq Shuffling
9 - With Freq Shuffling
C: SOP8 Package
P: Pb-free Package (norm if blank)
Y: Year Code(0-9)
WW: Week Code (01-52)
V: W/O OVP(norm if blank)

TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	GND	P	Ground
2	FB	I	Feedback input pin. PWM duty cycle is determined by voltage level into this pin and current-sense signal level at Pin 6.
3	VIN	I	Connected through a large value resistor to rectified line input for Start up chip supply and line voltage sensing.
4	RI	I	Internal Oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.
5	RT	I	Temperature sensing input pin. Connected through a NTC resistor to GND. Once the voltage of the RT pin drops below a fixed limit of 1.05V, PWM output will be disabled.
6	SENSE	I	Current sense input pin. Connected to MOSFET current sensing resistor node.
7	VDD	P	DC power supply pin.
8	GATE	O	Totem-pole gate drive output for power MOSFET.

BLOCK DIAGRAM



ESD INFORMATION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
HBM[Note]	Human Body Model	MIL-STD		2		KV
MM	Machine Model on All Pins	JEDEC-STD		250		V

Note: HBM all pins pass 2KV except VIN pin. The details are VIN passes 1kV, VDD and GATE pass 2KV, all other I/Os pass 8KV. In system application, VIN pin is either a high impedance input or left floating. The lower rating has minimum impacts on system ESD performance.

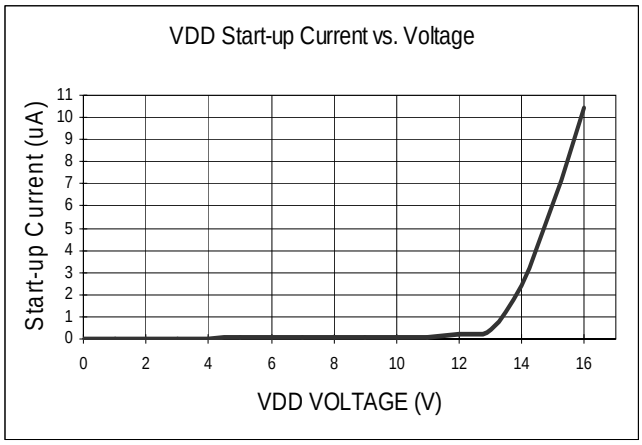
ELECTRICAL CHARACTERISTICS

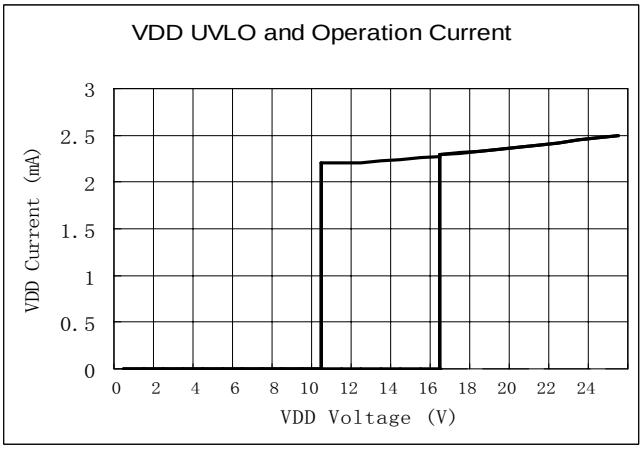
(T_A = 25^{O}C if not otherwise noted)

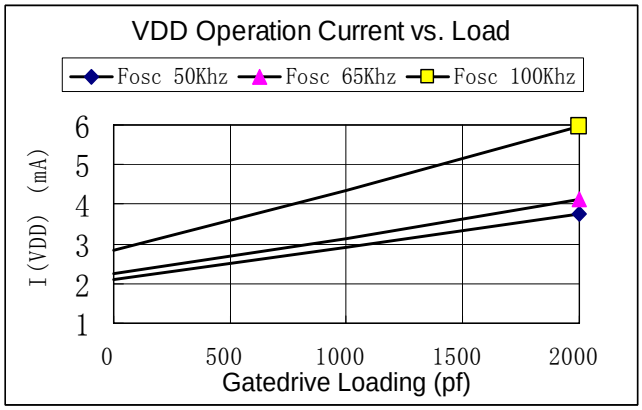
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD, VIN)						
I_V_{DD}_Startup	VDD Start up Current	VDD =15V, RI=100K Measure current into VDD		4	20	uA
I_V_{DD}_Operation	Operation Current	VDD=18V, RI=100Kohm, V_{FB}=3V, Gate floats		2.3		mA
UVLO(ON)	VDD Under Voltage Lockout Enter		9.5	10.5	11.5	V
UVLO(OFF)	VDD Under Voltage Lockout Exit (Recovery)		15.5	16.5	17.5	V
OVP(ON)*Optional	VDD Over Voltage Protection Enter		23.5	25	26.5	V
OVP(OFF)*Optional	VDD Over Voltage Protection Exit (Recovery)		21.5	23	24.5	V
OVP_Hysteresis	OVP(ON)-OVP(OFF)			2		V
T_D_OVP	VDD OVP Debounce time			80		uSec
V_{DD}_Clamp	V_{DD} Zener Clamp Voltage	I(V_{DD}) = 10 mA		35		V
Feedback Input Section(FB Pin)						
V_{FB}_Open	V_{FB} Open Loop Voltage			6.0		V
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND and measure current		0.65		mA
V_{TH}_BM	Burst Mode FB Threshold Voltage			1.8		V
V_{TH}_PL	Power Limiting FB Threshold Voltage			4.4		V
T_D_PL	Power limiting Debounce Time			80		mSec
Z_{FB}_IN	Input Impedance			9.0		Kohm
Current Sense Input(Sense Pin)						
T_blanking	Leading edge blanking time	RI = 100Kohm		400		ns
Z_{SENSE}_IN	Input Impedance			40		Kohm

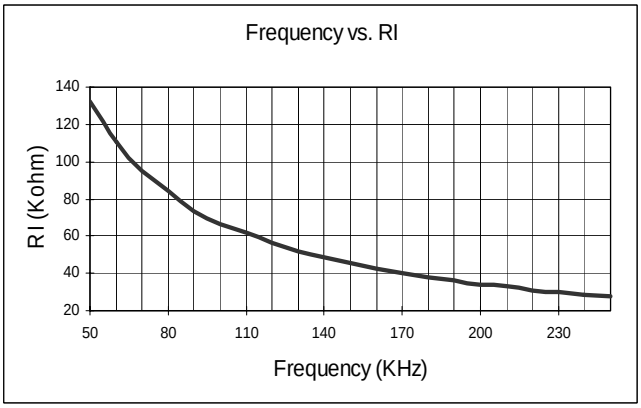
T_{D_OC}	Over Current Detection and Control Delay	From Over Current Occurs to GATE output turns off, Sense voltage ramp at 0.15V/uS.		120		nSec
V_{TH_OC}	Internal Current Limiting Threshold Voltage	VDD = 16V, I(VIN) = 55uA		0.86		V
Oscillator						
F_{OSC}	Normal Oscillation Frequency	RI = 100 Kohm	60	65	70	KHZ
Δf_Temp	Frequency Temperature Stability	VDD = 16V, RI = 100Kohm, 0°C to 85 °C		5		%
Δf_Volt	Frequency Voltage Stability	VDD = 15-25V, RI = 100Kohm		5		%
RI_range	Operating RI Range		50	100	250	Kohm
V_RI_open	RI open load voltage			2.0		V
F_BM	Burst Mode Base Frequency	VDD = 16V, RI = 100Kohm		22		KHZ
Gate Drive Output						
VOL	Output Low Level	VDD = 16V, Io = 20 mA			0.3	V
VOH	Output High Level	VDD = 16V, Io = 20 mA	11			V
VG_Clamp	Output Clamp Voltage Level			18		V
T_r	Output Rising Time	VDD = 16V, CL = 1nf		120		nSec
T_f	Output Falling Time	VDD = 16V, CL = 1nf		50		nSec
Over Temperature Protection						
I_RT	Output Current of RT pin	RI=100K		70		uA
V_{TH_OTP}	OTP Threshold Voltage		1.015	1.065	1.115	V
$V_{TH\_OTP\_off}$	OTP Recovery Threshold Voltage			1.165		V
T_{D_OTP}	OTP De-bounce Time			100		uSec
V_RT_Open	RT Pin Open Voltage	RI=100K		3.5		V
Frequency Shuffling (OB2269 Only)						
Δf_OSC	Frequency Modulation range /Base frequency	RI=100K	-5		5	%
f_Shuffling	Shuffling Frequency	RI=100K		65		HZ

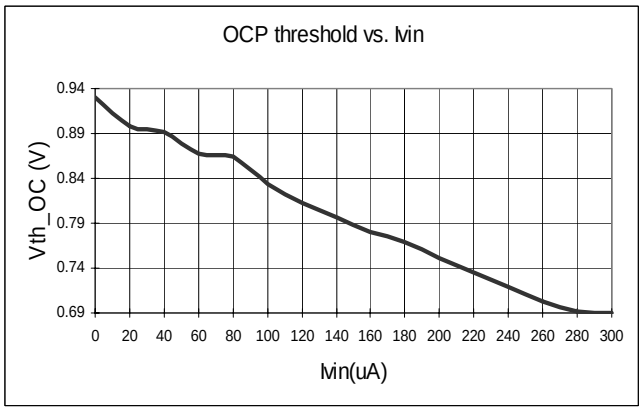
CHARACTERIZATION PLOTS











OPERATION DESCRIPTION

The OB2268/9 is a highly integrated PWM controller IC optimized for offline flyback converter applications in above 20W power range. The extended burst mode control greatly reduces the standby power consumption and helps the design easily meet the international power conservation requirements.

- **Startup Current and Start up Control**

Startup current of OB2268/9 is designed to be very low so that VDD could be charged up above UVLO threshold level and device starts up quickly. A large value startup resistor can therefore be used to minimize the power loss yet reliable startup in application. For AC/DC adaptor with universal input range design, a 2 MΩ, 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and yet low power dissipation design solution.

- **Operating Current**

The Operating current of OB2268/9 is low at 2.3mA. Good efficiency is achieved with OB2268/9 low operating current together with extended burst mode control schemes.

- **Frequency shuffling for EMI improvement**

The frequency Shuffling/jittering (switching frequency modulation) is implemented in OB2269. The oscillation frequency is modulated with a random source so that the tone energy is spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design.

- **Burst Mode Operation**

At zero load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy.
OB2268/9 self adjusts the switching mode according to the loading condition. At from no load to light/medium load condition, the FB input drops below burst mode threshold level (1.8V). Device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off state to minimize the switching loss thus reduce the standby power consumption to the greatest extend. The nature of high frequency switching also reduces the audio noise at any loading conditions.

- **Oscillator Operation**

A resistor connected between RI and GND sets the constant current source to charge/discharge the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation within the specified RI in Kohm range at nominal loading operational condition.

$$F_{PWM} = 6500/RI \ (KHZ)$$

- **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in OB2268/9 current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to Snubber diode reverse recovery so that the external RC filtering on sense input is no longer needed. The current limit comparator is disabled and cannot turn off the external MOSFET during the blanking period. The PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

- **Internal Synchronized Slope Compensation**

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

- **Over Temperature Protection**

An NTC resistor in series with a regular resistor should connect between RT and GND for temperature sensing and protection. NTC resistor value becomes lower when the ambient temperature rises. With the fixed internal current I_{RT} flowing through the resistors, the voltage at RT pin becomes lower at high temperature. The internal OTP circuit is triggered and shutdown the MOSFET when the sensed input voltage is lower than V_{TH}_OTP.

- **Gate Drive**

OB2268/9 Gate is connected to an external MOSFET gate for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI.
A good tradeoff is achieved through the built-in totem pole gate design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 18V clamp is added for MOSFET gate protection at higher than expected VDD input.

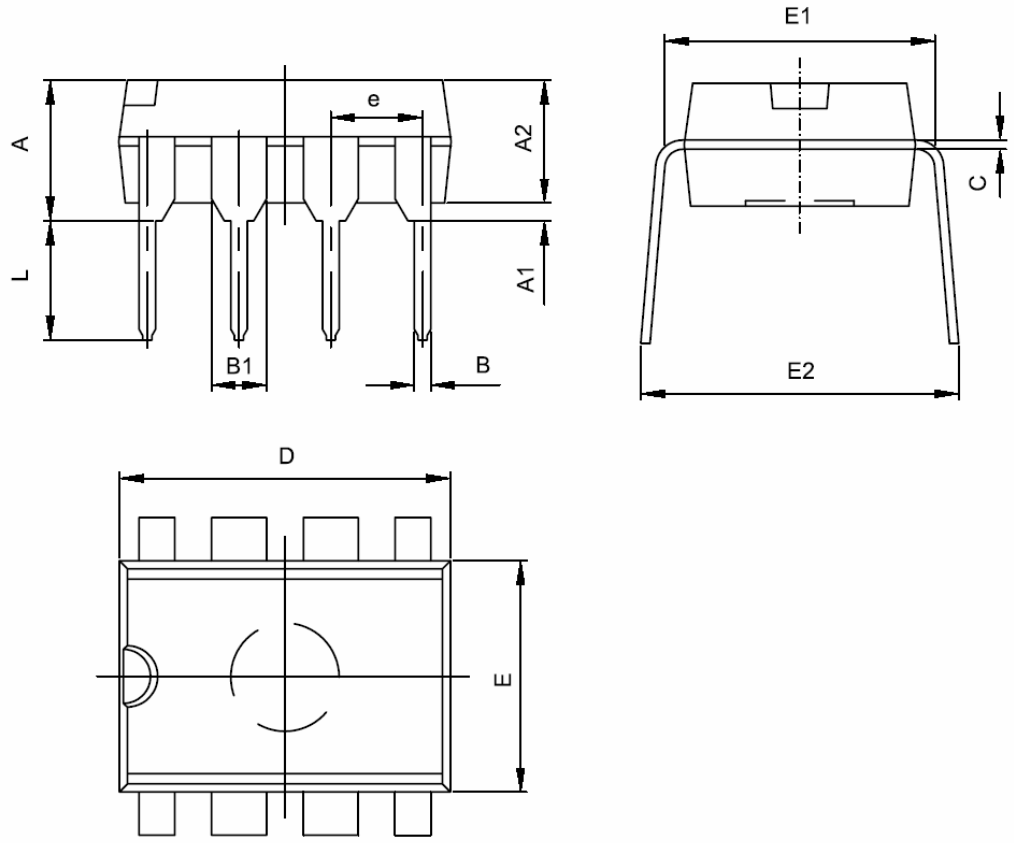
- **Protection Controls**

Good system reliability is achieved with OB2268/9's rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), over temperature protection (OTP), on-chip VDD over voltage protection (OVP, optional) and under voltage lockout.(UVLO).

The OCP threshold is input line voltage adjusted to compensate the increased output current limit at higher voltage caused by inherent Over-Current sensing and control delay. A constant output power limit is achieved with recommended reference design on OB2268/9.
At overload condition when FB input voltage exceeds power limit threshold value for more than 80mS, control circuit reacts to shut down the output power MOSFET. Device restarts when VDD voltage drops below UVLO limit.
Similarly, control circuit shuts down the power MOSFET when an Over Temperature condition is detected. OB2268/9 resumes the operation when temperature drops below the hysteresis value.
VDD is supplied with transformer auxiliary winding output. It is clamped when VDD is higher than 30V. The power MOSFET is shut down when VDD drops below UVLO limit and device enters power on start-up sequence thereafter.

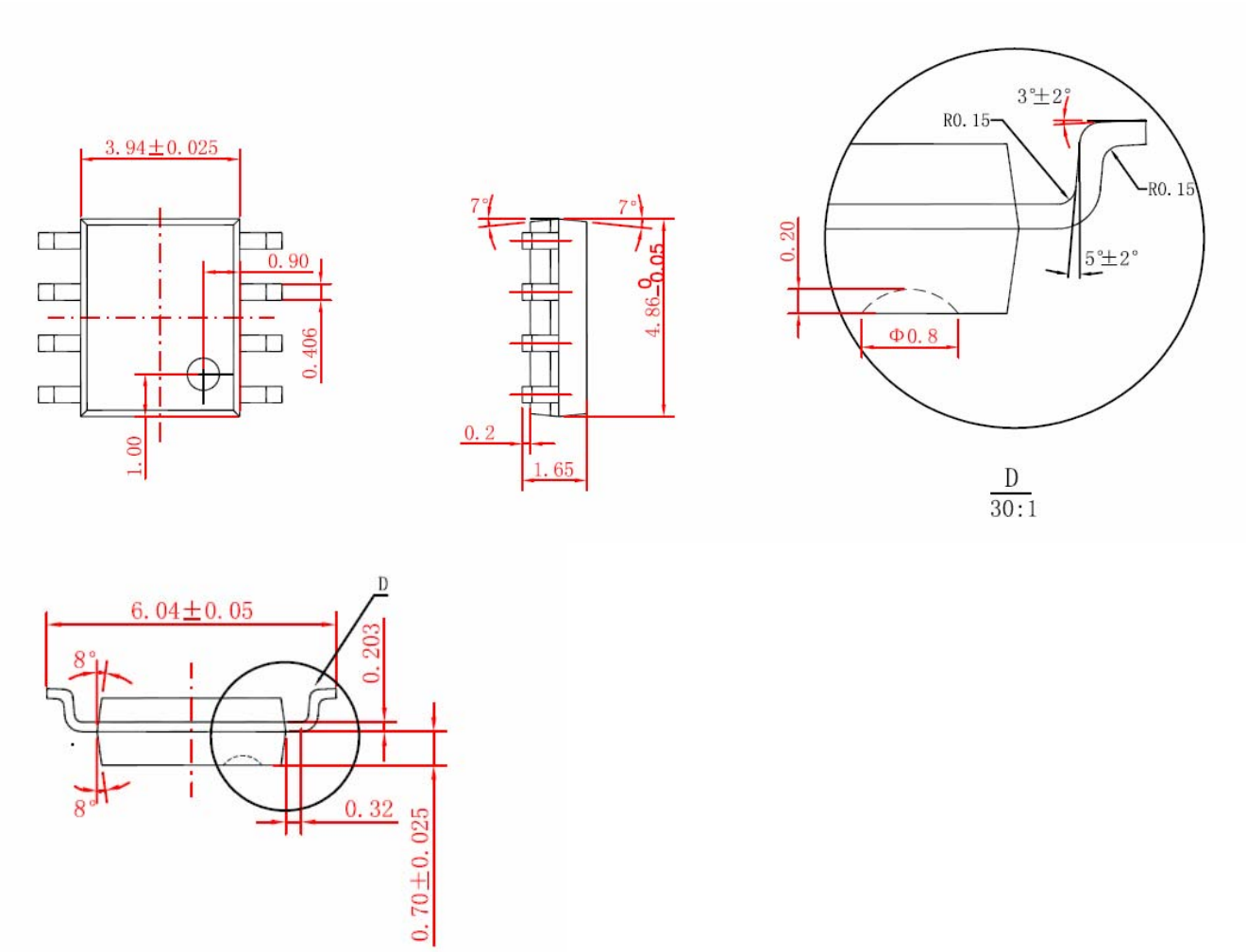
PACKAGE MECHANICAL DATA

8-Pin Plastic DIP



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.360	0.560	0.014	0.022
B1	1.524(TYP)		0.060(TYP)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.620(TYP)		0.300(TYP)	
e	2.540(TYP)		0.100(TYP)	
L	3.000	3.600	0.118	0.142
E2	8.200	9.400	0.323	0.370

8-Pin Plastic SOP



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