JW5143/JW5143P

100V, 3.5A Current Limit Async. Step-Down Converter with Low IQ

DESCRIPTION

The JW5143 and JW5143P are monolithic buck switching regulators based on COT architecture. Operating with an input range of 6V~100V, JW5143 and JW5143P integrate high-side N-Channel MOSFET with a peak current limit of 3.5A. At light loads, the regulator operates in low frequency to maintain high efficiency.

JW5143 and JW5143P guarantee robustness with output short protection, thermal protection, current run-away protection, input under voltage lockout.

JW5143 and JW5143P are available in ESOP-8 package, which provide a compact solution with minimal external components.

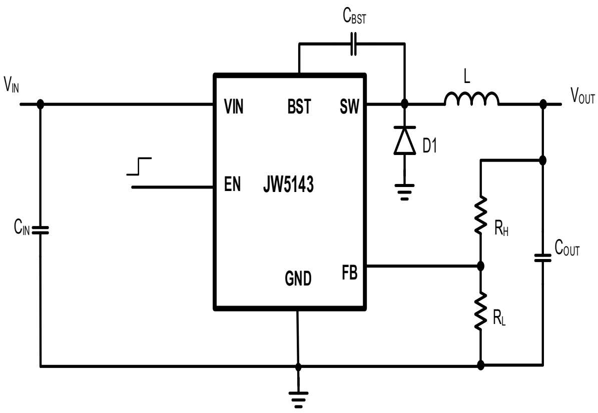
FEATURES

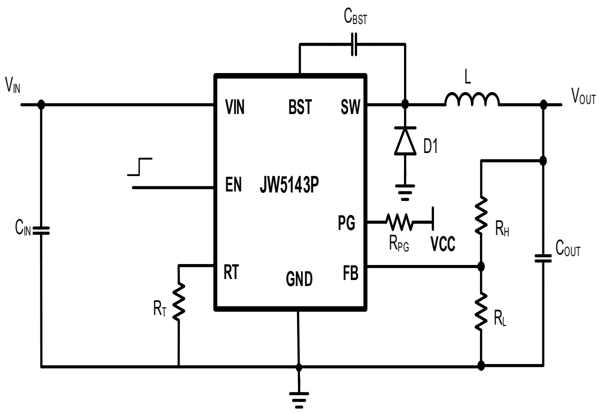
- 6V to 100V Operating Input Range
- 3.5A Peak Current Limit
- Very Low Quiescent Current: 20uA
- Fixed 300kHz Switching Frequency (JW5143)
- Adjustable Switching Frequency from 100kHz to 600kHz (JW5143P)
- Input Under Voltage Lockout
- Current Run-away Protection
- Output Short Protection
- Thermal Protection
- Available in ESOP-8 Package

APPLICATIONS

- GPS Tracker
- E-bike
- Telecom/Networking Power

TYPICAL APPLICATION

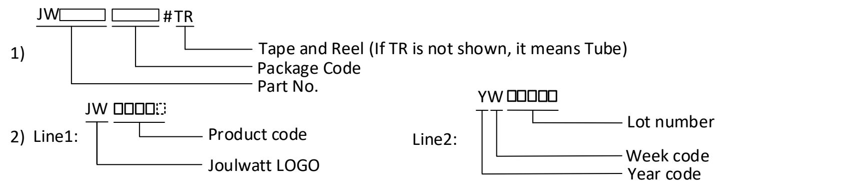




ORDER INFORMATION

DEVICE[1)]	PACKAGE	TOP MARKING[2)]	ENVIRONMENTAL[3)]
JW5143ESOP#TR	ESOP8	JW5143 YW□□□□□	Green
JW5143PESOP#TR	ESOP8	JW5143P YW□□□□□	Green

Notes:



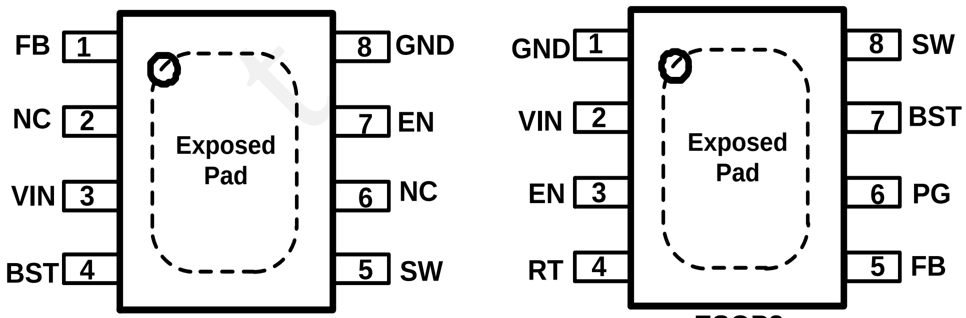
3) All Joulwatt products are packaged with Pb-free and Halogen-free materials and compliant to RoHS standards.

DEVICE INFORMATION

DEVICE	Adjustable switching frequency	Function
JW5143ESOP#TR	NO	-
JW5143PESOP#TR	YES	PG

PIN CONFIGURATION

TOP VIEW



ESOP8 JW5143 ESOP8 JW5143P

ABSOLUTE MAXIMUM RATING[1)]

VIN ………... -0.3V to 110V
SW ……….. -0.6V (-8V for 10ns) to 110V
PG……………………………………………………………………………………………… -0.3V to 14V
BST Pin .... SW-0.3V to SW+6V
All other Pins .... -0.3V to 6V
Junction Temperature [2)] 150ºC
Lead Temperature ....260℃
Storage Temperature ....-65ºC to +150ºC
ESD Susceptibility (Human Body Model) 2kV
ESD Susceptibility (Charged Device Model) 500V

RECOMMENDED OPERATING CONDITIONS[3)]

Input Voltage VIN ....6V to 100V
Continues Output Current 1.5A
Output Voltage V_{OUT}...1.2V to Dmax*VIN
Junction Temperature Range ....-40ºC to 125℃
Ambient Temperature Range ....-40ºC to 85℃

THERMAL PERFORMANCE[4)]

	θ_{JA}	θ_{Jc}	
ESOP8	45	6	ºC/W

Notes:

1) Exceeding these ratings may damage the device. These stress ratings do not imply function operation of the device at any other conditions beyond those indicated under RECOMMENDED OPERATING CONDITIONS.
2) The JW5143P series includes thermal protection that is intended to protect the device in overload conditions. Continuous operation over the specified absolute maximum operating junction temperature may damage the device.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS

V_{IN}=48V, T_A=25℃，Unless otherwise stated..

ITEM	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
V_{IN} Under Voltage Lock-out Threshold	V_{IN_UVLO}	V_{IN} rising	5.3	5.6	5.9	V
V_{IN} Under voltage Lockout Hysteresis	V_{IN_HYS}			150		mV
Shutdown Supply Current	I_{SD}	V_{EN}=0V			2	μA
Supply Current	I_Q	V_{EN}=3V, V_{FB}=1.4V		20	30	μA
Feedback Voltage	V_{FB}	V_{IN}=48V, TA=25℃	1.207	1.225	1.243	V
Top Switch Resistance[5)]	$R_{DS(ON)T}$			550		mΩ
Top Switch Leakage Current	I_{LEAK_TOP}	V_{IN}=48V, V_{EN}=0V, V_{SW}=0V			1	μA
Top Switch Current Limit			3	3.5	4	A
Current Limit Forced Off Time		V_{IN}=12V, V_{FB}=1.1V		750		ns
		V_{IN}=48V, V_{FB}=0V		54.4		us
Centre Switching Frequency	Fsw	JW5143, VOUT=12V, IOUT=1A		300		kHz
		R_T=60kΩ, JW5143P, VOUT=12V, IOUT=1A		500		kHz
		R_T=100kΩ, JW5143P, VOUT=12V, IOUT=1A		300		kHz
		R_T=150kΩ, JW5143P, VOUT=12V, IOUT=1A		200		kHz
Switching Frequency Range	Fsw		100		600	kHz
Minimum On Time[5)]	T_{ON_MIN}			110	160	ns
Maximize On Time[5)]	T_{ON_MAX}			6	7.5	us
Minimum Off Time	T_{OFF_MIN}			200	250	ns
EN Shut Down Threshold Voltage	V_{EN_Rise}	V_{EN} rising	1.15	1.225	1.27	V
	V_{EN_HYS}	Hysteresis Voltage		200		mV
	I_{EN}	Pull high current		240		nA
Soft-Start	t_{SS}	10%V_{OUT}~90%V_{OUT}		1.5		ms
Power Good Lower Threshold	PG_{LTH}	FB rising (JW5143P)	87.5%	90%	92.5%	V_{REF}
		FB falling (JW5143P)	77.5%	80%	82.5%	V_{REF}
Power Good Upper Threshold	PG_{UTH}	FB rising (JW5143P)	112.5 %	115%	117.5 %	V_{REF}
		FB falling (JW5143P)	107.5 %	110%	112.5 %	V_{REF}

Power Good Output High Leakage	I_{PG_LEAK}	V_{PG} = 14 V, TA = 25°C (JW5143P)			100	nA
Power Good Low State Output Voltage	V_{PG}	V_{FB} = 2 V, I_{PG} = 2 mA (JW5143P)			0.3	V
Power Good Delay Time	$PGD_{\_DLY}$	(JW5143P)		13		us
Thermal Shutdown[5)]	T_{TSD}			165		°C
Thermal Shutdown hysteresis[5)]	T_{TSD_HYS}			20		°C
OC Hiccup Wait Time[5)]				128		Cycle
OC Hiccup Time before Start[5)]			7	9	12	ms

Note :

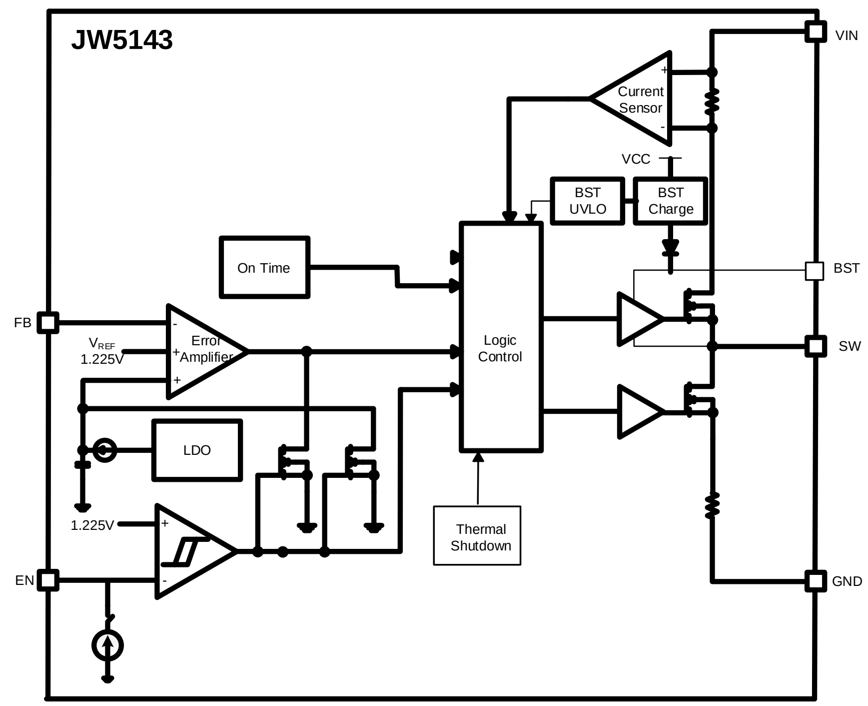
5) Guaranteed by design.

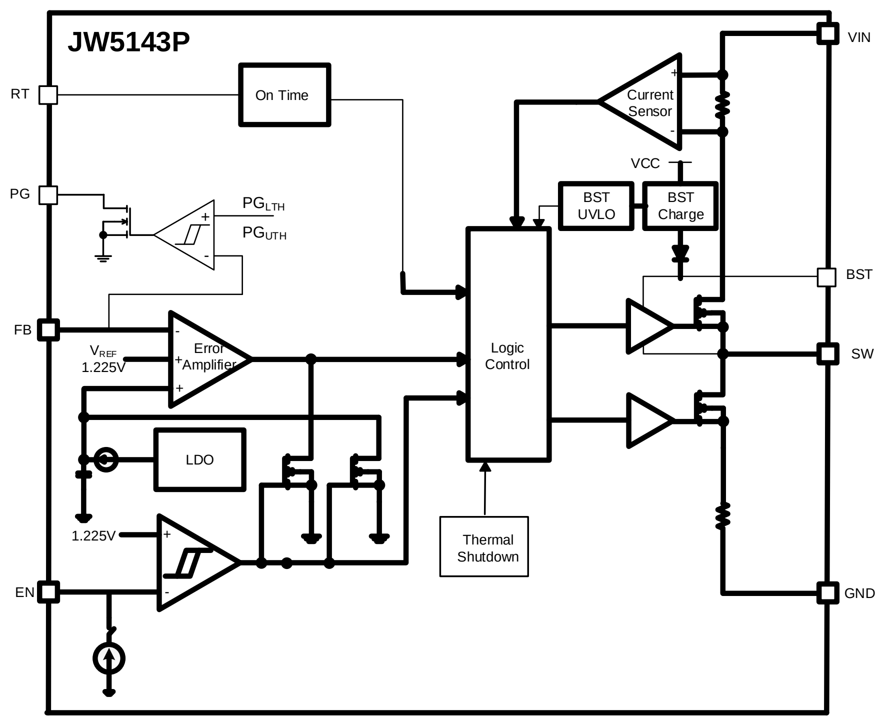
PIN DESCRIPTION

PIN JW5143	NAME	DESCRIPTION
1	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 1.225 V. Connect a resistive divider at FB.
2	NC	Not connected.
3	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 6V to 100V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
4	BST	Connect a 0.1uF capacitor between BST and SW pin to supply current for the top switch driver.
5	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
6	NC	Not connected.
7	EN	This is Enable pin. Float the EN to enable. And internal has one zero diode that allow EN can be pull high to VIN via a resistor. The resistor should be larger than 50kΩ.
8	GND	Ground Pin
Exposed Pad		For proper operation, connect the GND pin to the exposed thermal part. This thermal pad should be connected to any internal PCB ground plane using multiple vias for good thermal performance.

PIN JW5143P	NAME	DESCRIPTION
1	GND	Ground Pin
2	VIN	Input voltage pin. VIN supplies power to the IC. Connect a 6V to 100V supply to VIN and bypass VIN to GND with a suitably large capacitor to eliminate noise on the input to the IC.
3	EN	This is Enable pin. Float the EN to enable. And internal has one zero diode that allow EN can be pull high to VIN via a resistor. The resistor should be larger than 50kΩ.
4	RT	Switching frequency program input. Connect a resistor from this pin to GND to set the switching frequency.
5	FB	Output feedback pin. FB senses the output voltage and is regulated by the control loop to 1.225 V. Connect a resistive divider at FB.
6	PG	Power good open drain output. Connect a pull-up resistor with this pin
7	BST	Connect a 0.1uF capacitor between BST and SW pin to supply current for the top switch driver.
8	SW	SW is the switching node that supplies power to the output. Connect the output LC filter from SW to the output load.
Exposed Pad		For proper operation, connect the GND pin to the exposed thermal part. This thermal pad should be connected to any internal PCB ground plane using multiple vias for good thermal performance.

BLOCK DIAGRAM

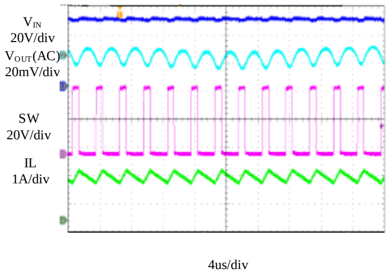




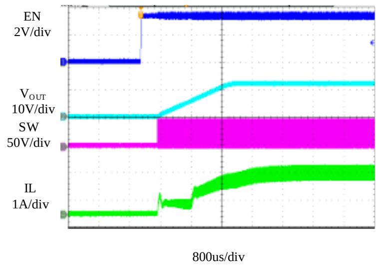
TYPICAL PERFORMANCE CHARACTERISTICS

JW5143, V_{IN} =48V, V_{OUT}= 12V, L =68µH, COUT = 50µF, R_T = 249KΩ, T_A = +25°C, unless otherwise noted

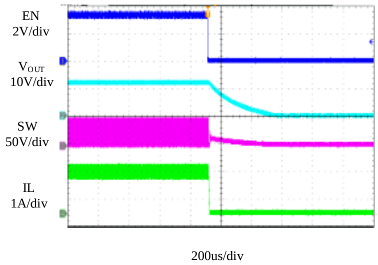
Steady State Test
V_{IN}=48V, V_{OUT}=12V
I_{OUT}=1.5A



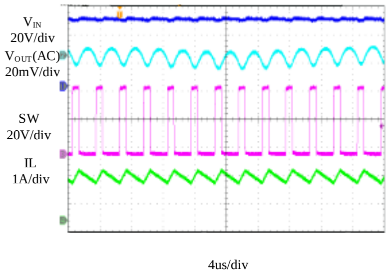
Startup through Enable
V_{IN}=48V, V_{OUT}=12V
I_{OUT}=1.5A (Resistive load)



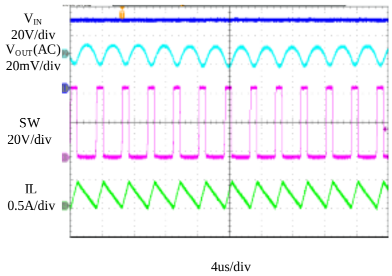
Shutdown through Enable
V_{IN}=48V, V_{OUT}=12V
I_{OUT}=1.5A (Resistive load)



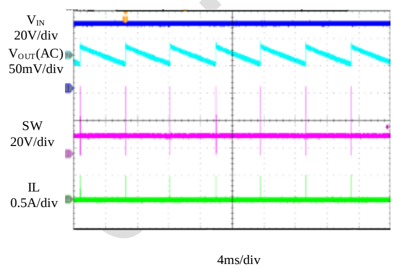
Heavy Load Operation
1.5A LOAD



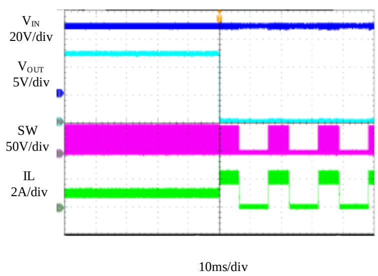
Light Load Operation
0.2A LOAD



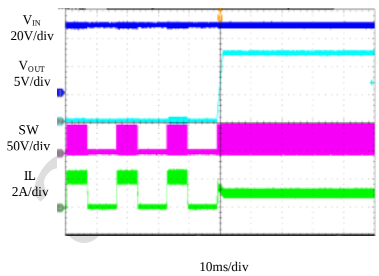
No Load Operation
0 A LOAD



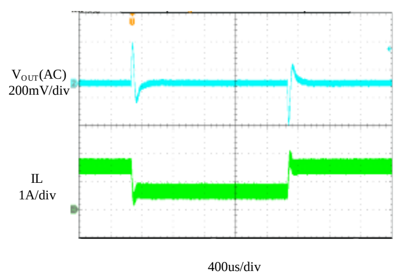
Short Circuit Protection
V_{IN}=48V, V_{OUT}=12V
I_{OUT}=1A-Short



Short Circuit Recovery
V_{IN}=48V, V_{OUT}=12V
I_{OUT}= Short-1A



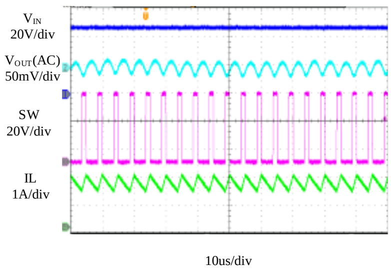
Load Transient
1.5A LOAD->0.6A LOAD->1.5A LOAD



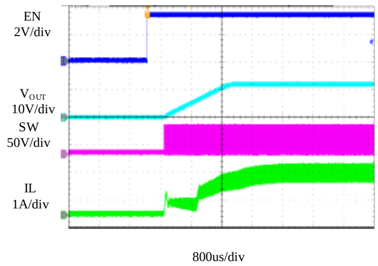
TYPICAL PERFORMANCE CHARACTERISTICS(continued)

JW5143P, V_{IN} =48V, V_{OUT}= 12V, L =100μH, COUT = 50μF, R_T = 150kΩ, T_A = +25°C, unless otherwise noted

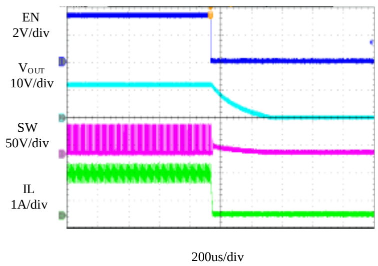
Steady State Test
V_{IN}=48V, V_{OUT}=12V
I_{OUT}=1.5A



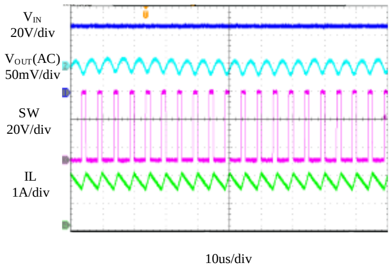
Startup through Enable
V_{IN}=48V, V_{OUT}=12V
I_{OUT}=1.5A (Resistive load)



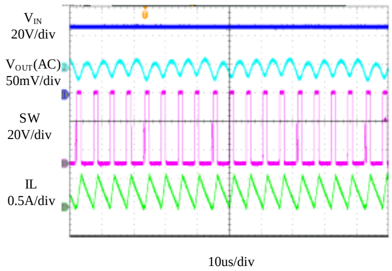
Shutdown through Enable
V_{IN}=48V, V_{OUT}=12V
I_{OUT}=1.5A (Resistive load)



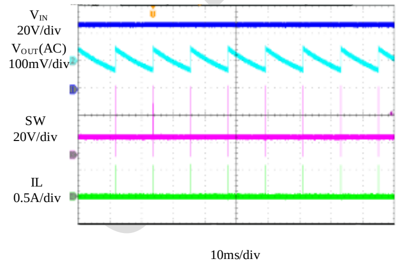
Heavy Load Operation
1.5A LOAD



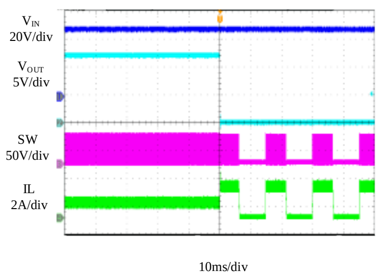
Light Load Operation
0.26A LOAD



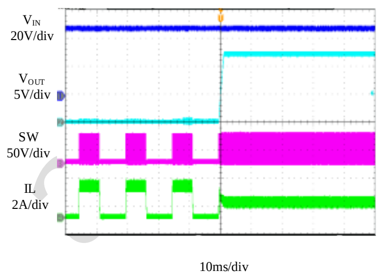
No Load Operation
0 A LOAD



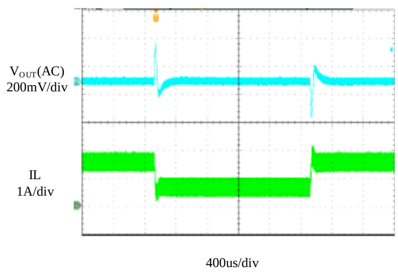
Short Circuit Protection
V_{IN}=48V, V_{OUT}=12V
I_{OUT}=1A-Short



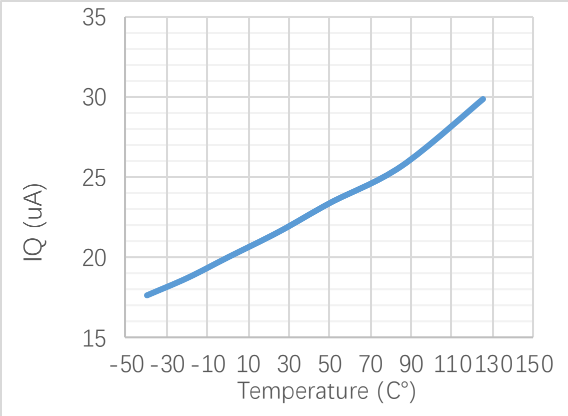
Short Circuit Recovery
V_{IN}=48V, V_{OUT}=12V
I_{OUT}= Short-1A



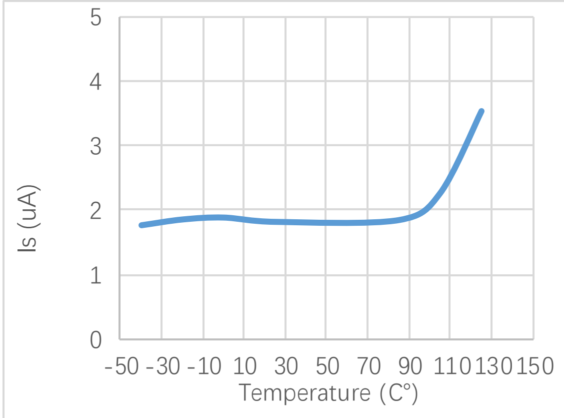
Load Transient
1.5A LOAD->0.6A LOAD->1.5A LOAD



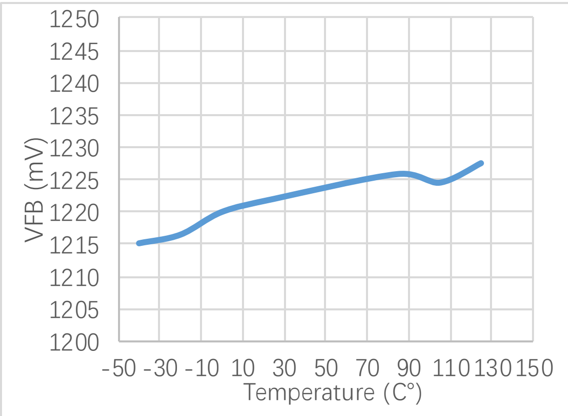
TYPICAL PERFORMANCE CHARACTERISTICS(continued)



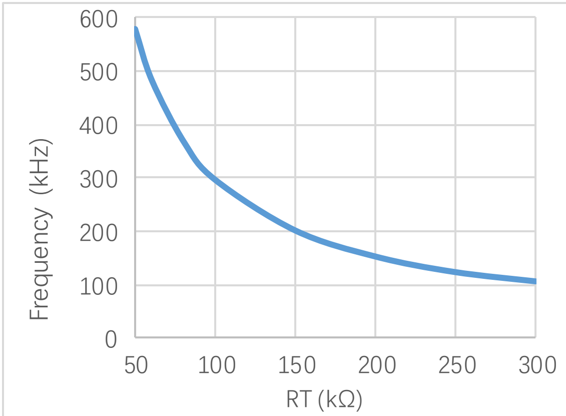
Supply Current vs Junction Temperature



Shutdown Current vs Junction Temperature

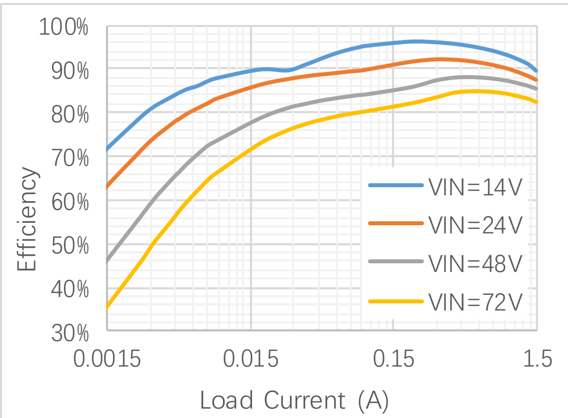


FB Voltage Regulaion vs Junction Temperature



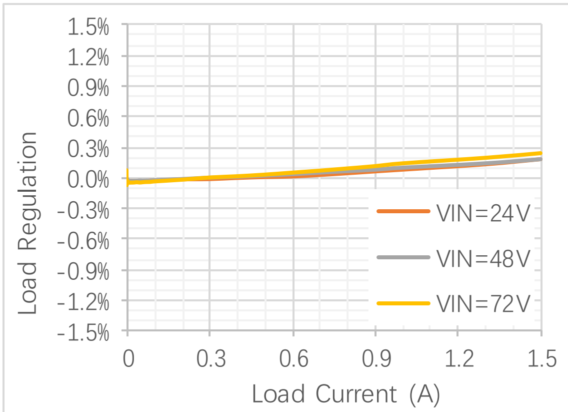
Switch Frequency vs RT

(JW5143P, V_{OUT}=12V, I_{OUT}=1A)



Efficiency vs Load Current

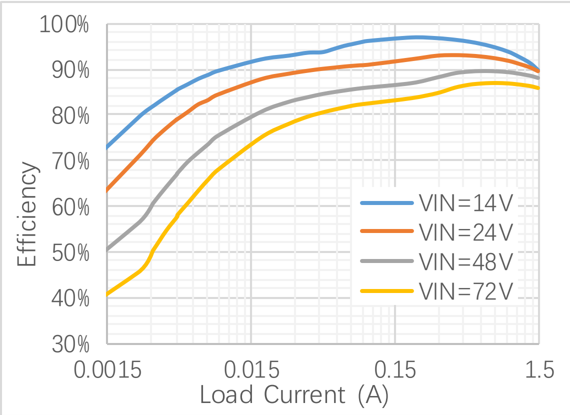
(JW5143, V_{OUT}=12V, L=68μH)



Load Regulation vs Load Current

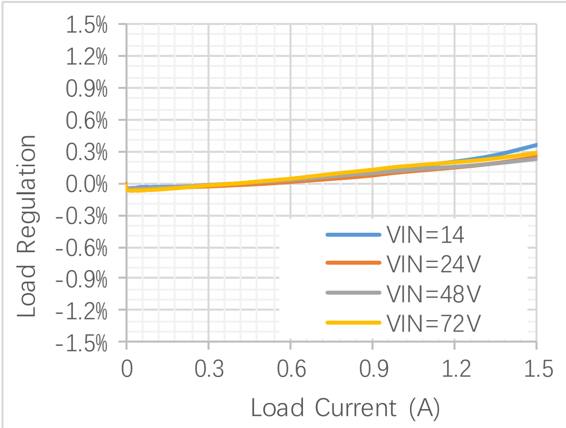
(JW5143, V_{OUT}=12V, L=68μH)

TYPICAL PERFORMANCE CHARACTERISTICS(continued)



Efficiency vs Load Current

(JW5143P, V_{OUT}=12V, L=100μH, R_T=150k)



Load Regulation vs Load Current

(JW5143P, V_{OUT}=12V, L=100μH, R_T=150k)

FUNCTIONAL DESCRIPTION

The JW5143 and JW5143P are asynchronous, COT step-down regulators. They regulate input voltages from 6V to 100V down to an output voltage as low as 1.225V, and is capable of supply up to 1.5A continuous, 3.5A transient of load current.

Constant On-Time Control and PWM Operation

The main control loop of JW5143 and JW5143P are constant on-time pulse width modulation (PWM) controllers that combine adaptive on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count-configuration with both low-ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This is MOSFET is turned off after internal one shot timer expires. Once the feedback voltage falls below the reference voltage, the high-side MOSFET is turned on again. An internal ramp is added to reference voltage to simulate the ripple, eliminate the need for output ripple from this COT control.

Switching Frequency (JW5143P)

The switching frequency of JW5143P can be programmed by the resistor RT from RT pin to GND. In a typical application scenario with an input voltage of 48V, an output voltage of 12V and a load of 1A, the frequency can be calculated by the following equation:

$$F_{SW}(kHz) = \frac{30000}{RT(k\Omega)}$$

To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the conversion efficiency, maximum input voltage and minimum controllable on time should be considered. The minimum controllable on time is typically 150ns which limit the maximum operating frequency in applications with high input to output step down ratios.

Enable and Adjusting Under-Voltage Lockout

The EN pin provides electrical on and off control of the device. When the EN pin exceeds the threshold voltage, the device begins operating. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching.

The EN pin has internal pull-up current source which allows the user to float the EN pin to enable device. If an application requires control of the EN pin, open-drain or open-collector output logic can be used to interface with the pin.

The JW5143 and JW5143P implement internal under-voltage-lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal V_{IN} UVLO threshold. The internal V_{IN} UVLO threshold has a hysteresis of 150mV.

If an application requires a higher V_{IN} under-voltage lockout (UVLO) threshold, use a resistive divider connected between VIN and ground with the central tap connected to EN to adjust the input voltage UVLO. (Shown in Figure 1). So that when V_{IN} rises to the pre-set value, EN rises above 1.225V to enable the device and when V_{IN} drops below the pre-set value, EN drops below 1.025V to trigger input under voltage lockout protection.

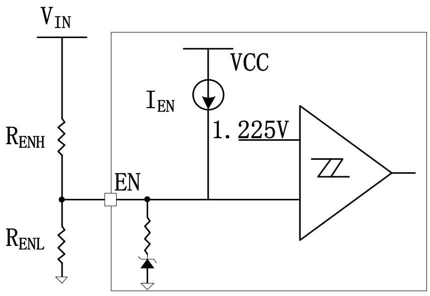


Figure1. Adjustable UVLO

$$V_{UVLO} = \frac{R_{ENH} + R_{ENL}}{R_{ENL}} * (V_{EN\_Rise} - I_{EN} * \frac{R_{ENH} * R_{ENL}}{R_{ENH} + R_{ENL}})$$

$$V_{UVLO\_HYS} = \frac{R_{ENH} + R_{ENL}}{R_{ENL}} * V_{EN\_HYS}$$

Where V_{EN_Rise}=1.225V, V_{EN_HYS}=200mV and I_{EN}=200nA.

Low Dropout Operating and Bootstrap Voltage

The JW5143 and JW5143P integrate an N-channel buck switch and associated floating high-side gate driver. The gate-driver circuit works in conjunction with and external bootstrap capacitor and an internal high-voltage bootstrap diode. A 0.1uF or larger ceramic capacitor connected between the BST pin and the SW pin provides the voltage to the high-side driver during buck switch ON time. During the OFF time as the SW node is pulled down, and the bootstrap capacitor charges from internal VCC through the internal bootstrap diode.

When operating with a low voltage difference from input to output, the high-side MOSFET will operate at approximate 97% duty cycle. When the high-side MOSFET is continuously on some switching cycles, the voltage from BST to SW drops below BST UVLO threshold 2.1V, the high-side MOSFET is turned off immediately and an integrated low side MOSFET pulls SW low to recharge the BOOT capacitor with the 200ns (typ.) min-off time.

Since the gate drive current sourced from the BOOT capacitor is small, the high-side MOSFET can remain on for many switching cycles before the MOSFET is turned off to refresh the capacitor. Thus the effective duty cycle of the switching regulator can be high, approaching 97%. The effective duty cycle of the converter during dropout is mainly influenced by the voltage drops across the power MOSFET, the inductor resistance, the low side diode voltage and the printed circuit board resistance.

Output Short Protection

The JW5143 and JW5143P provide an intelligent current limit OFF timer that adjusts the OFF time to reduce fold-back of current limit. If the peak value of the current in the buck switch exceeds high side current limit, the present ON-time period is immediately terminated, and a non-resettable OFF timer is initiated. The length of the OFF time is controlled by the V_{OUT} and the input voltage V_{IN}. For example, V_{IN}=48V and V_{OUT}=0V, the OFF time is set to 54.4us (typ.). This condition occurs if the output is shorted or during initial phases of start up. In case of output overload where the FB voltage is greater than zero volts (a soft short), the current limit OFF time is reduced. The current limit OFF time T_{OFF} is calculated by below equation.

$$T_{OFF}(s) = 3 * 10^{-12} \frac{A}{B}$$

$$A = 0.5 + \frac{V_{IN} - 10}{60}$$

$$B = \mathrm{Min}\left\{\left(2 * 10^{-6} - \frac{6 - V_{OUT}}{3.125 * 10^{6}}\right), \left(\frac{V_{FB}}{390 * 10^{3}} + 62.5 * 10^{-9}\right)\right\}$$

Furthermore, if an output overload condition occurs for more than the hiccup wait time, which is programmed for 128 switching cycles, the devices shuts down and re-starts after hiccup time 9ms. This hiccup mode helps to reduce the device power dissipation under severe over current conditions.

Power Good (JW5143P)

The JW5143P has power-good (PG) output. The PG pin is one open drain. Connect to a voltage source (such as VOUT) through a resistor. When the output voltage becomes within +/-10% of the target value, internal comparators detect power good state and power good signal becomes high. If the feedback voltage goes under or higher +/-15% of the target value, the power good signal becomes low.

Thermal Protection

When the temperature of the JW5143 and JW5143P rise above 165°C, they are forced into thermal shut-down. Only when the core temperature drop below 145°C can allow the regulators become active again.

APPLICATION INFORMATION

Output Voltage Set

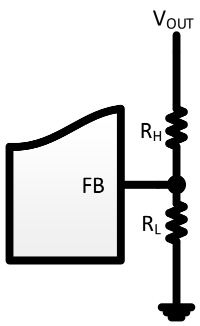
The output voltage is determined by the resistor divider connected at the FB pin, and the voltage ratio is:

$$V_{FB} = V_{OUT} * \frac{R_L}{R_H + R_L}$$

where V_{FB} is the feedback voltage and V_{OUT} is the output voltage.

Choose R_L around 1 kΩ~20kΩ, and then R_H can be calculated by:

$$R_H = R_L * \left(\frac{V_{OUT}}{1.225} - 1\right)$$



Feedforward Capacitor

In order to improve dynamic performance, a feedforward capacitor (C_{FF}) can be considered to be in parallel with R_H.

Input Capacitor

The input capacitor is used to supply the AC input current to the step-down converter and maintain the DC input voltage. Estimate the RMS current in the input capacitor with:

$$I_{CIN} = I_{OUT} * \sqrt{\frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

where I_{OUT} is the load current, V_{OUT} is the output voltage, V_{IN} is the input voltage.

The input capacitor can be calculated by the following equation when the input ripple voltage is determined.

$$C_{IN} = \frac{I_{OUT}}{F_{SW} * \Delta V_{IN}} * \frac{V_{OUT}}{V_{IN}} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where C_{IN} is the input capacitance value, F_{SW} is the switching frequency, $\triangle V_{IN}$ is the input ripple voltage.

The input capacitor can be electrolytic, tantalum or ceramic. To minimize the potential noise, a small X5R or X7R ceramic capacitor, e.g. 0.1μF, should be placed as close to the IC as possible when using electrolytic capacitors.

A 22μF/200V electrolytic capacitor is recommended in typical application.

Output Capacitor

The output capacitor is required to maintain the DC output voltage, and the capacitance value determines the output ripple voltage. The output voltage ripple can be calculated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{F_{SW} * L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right) * \left(R_{ESR} + \frac{1}{8 * F_{SW} * C_{OUT}}\right)$$

where C_{OUT} is the output capacitance value and R_{ESR} is the equivalent series resistance value of the output capacitor.

The output capacitor can be low ESR electrolytic, tantalum or ceramic, and lower ESR capacitors get lower output ripple voltage.

The output capacitors also affect the system stability and transient response, and a 44μF~66μF ceramic capacitor is recommended in typical application.

Inductor

The inductor is used to supply constant current to the output load, and the value determines the ripple current which affect the efficiency and the output voltage ripple. The ripple current is typically allowed to be 40% of the maximum switch current limit, thus the inductance value can be calculated by:

$$L = \frac{V_{OUT}}{F_{SW} * \Delta I_L} * \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

where V_{IN} is the input voltage, V_{OUT} is the output voltage, F_{SW} is the switching frequency, and $\triangle I_L$ is the peak-to-peak inductor ripple current.

External Bootstrap Capacitor

A bootstrap capacitor is required to supply voltage to the top switch driver. A 0.1μF low ESR ceramic capacitor is recommended to be connected between the BST pin and SW pin.

External Diode

The JW5143 and JW5143P require an external catch diode between the SW pin and GND. The selected diode must have a reverse voltage rating equal to or greater than VIN(max). The peak current rating of the diode must be greater than the maximum inductor current.

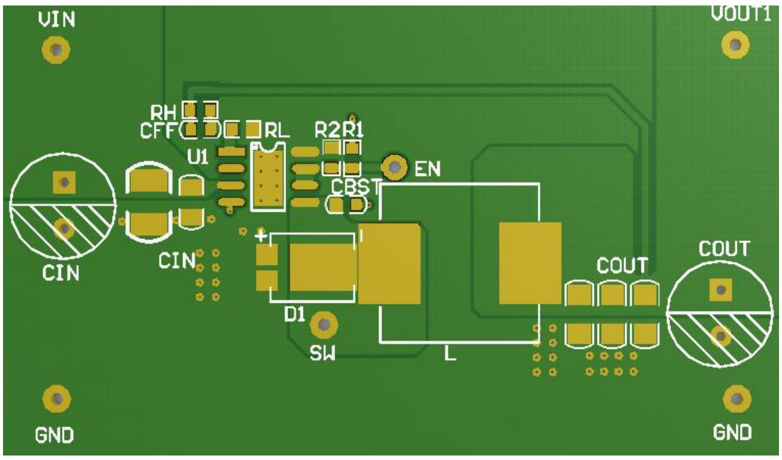
The catch diode must be Schottky diodes. The lower the forward voltage of the diode, the higher the efficiency of the regulator. Typically, diodes with higher voltage and current ratings have higher forward voltages. From the perspectives of efficiency and safety, the forward voltage of the Schottky diode should not exceed 1V.

PCB Layout Note

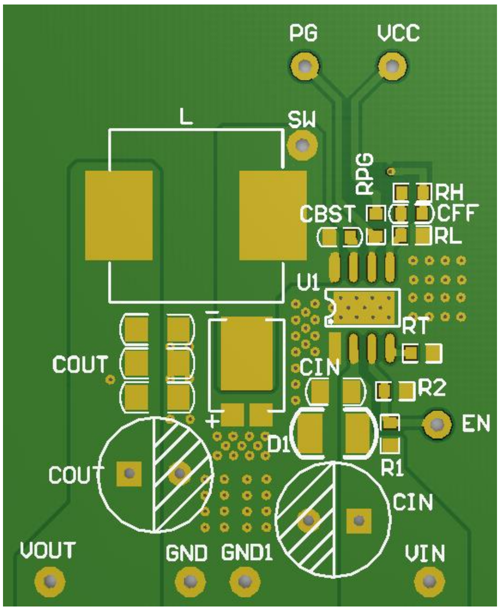
For minimum noise problem and best operating performance, the PCB is preferred to following the guidelines as reference.

1. Place the input decoupling capacitor as close to JW5143/P (VIN pin and PGND) as possible to eliminate noise at the input pin. The loop area formed by input capacitor and GND must be minimized.
2. Put the feedback trace as short as possible, and far away from the inductor and noisy power traces like SW node.
3. The ground plane on the PCB should be as large as possible for better heat dissipation.
4. Keep the switching node SW short to prevent excessive capacitive coupling
5. Make V_{IN}, V_{OUT} and ground bus connections as wide as possible. This reduces any voltage drops on the input or output paths of the converter and maximizes efficiency.

ESOP8:



JW5143 PCB Layout Recommendation



JW5143P PCB Layout Recommendation

REFERENCE DESIGN

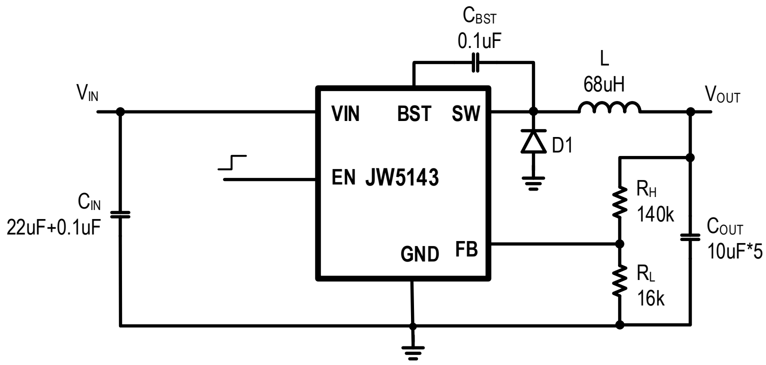
Note: Information in the following reference design sections is not part of JoulWatt component specification. Customers are responsible for determining suitability of components chosen for their purposes and should validate their design implementation to make sure the proper system functionality.

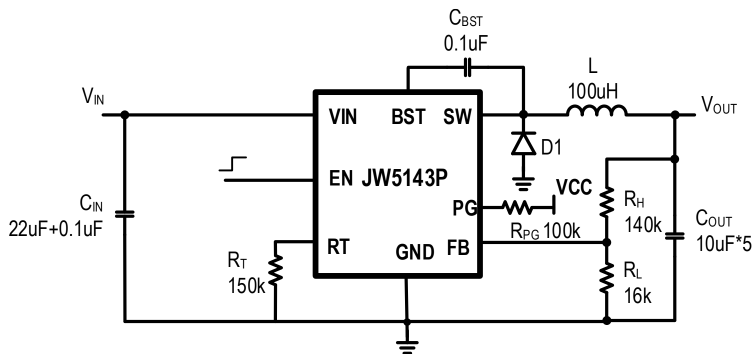
Reference 1:

V_{IN}: 15V~100V

V_{OUT}: 12V

I_{LOAD}: 0~1.5A



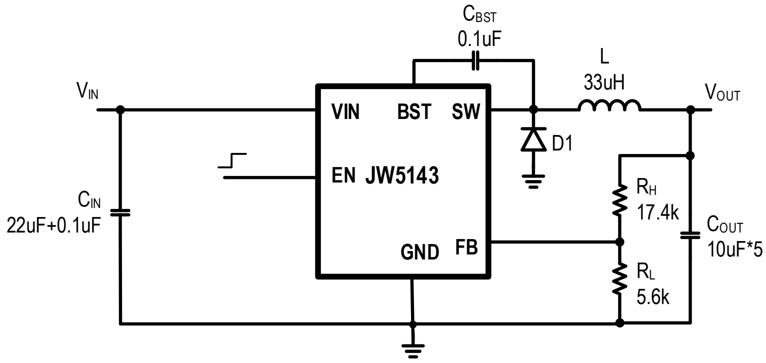


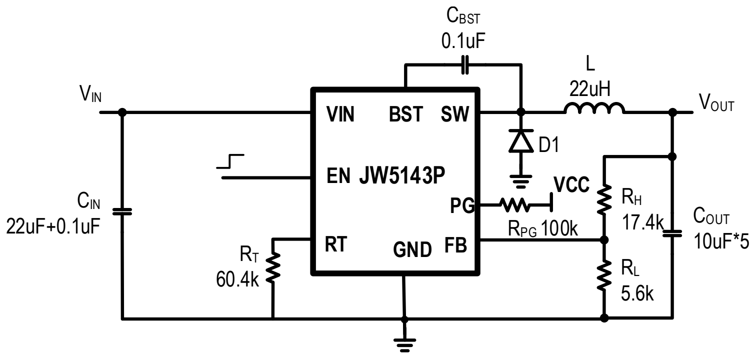
Reference 2:

V_{IN}: 9V~100V

V_{OUT}: 5V

I_{LOAD}: 0~1.5A





External Components Suggestion (V_{IN}=48V):

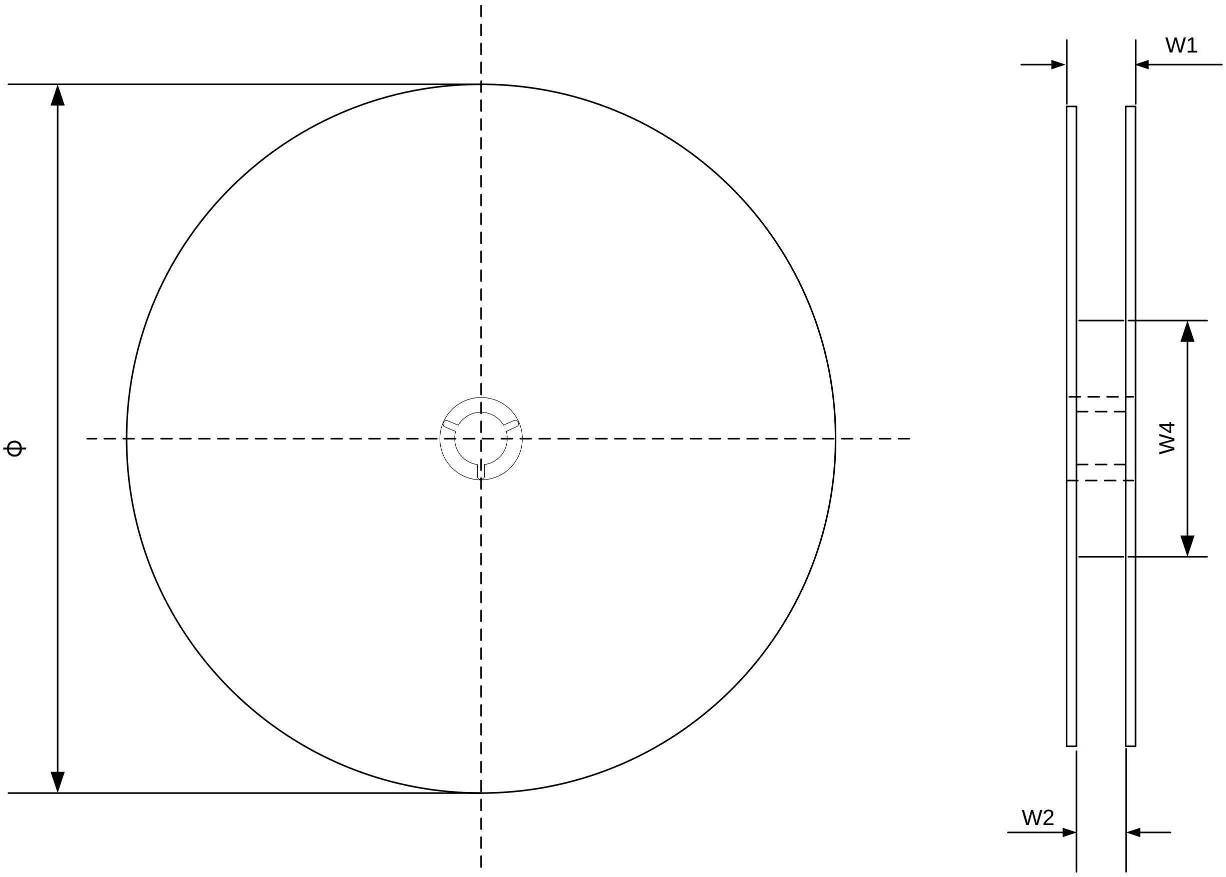
Device	V_{OUT}(V)	R_H (kΩ)	R_L (kΩ)	R_T (kΩ)	L (μH)	C_{OUT_NOM} (μF)	C_{OUT_EFF} (μF)
JW5143	12	140	16	-	68	50	30
JW5143P	12	140	16	150	100	50	30
JW5143	5	17.4	5.6	-	33	50	35
JW5143P	5	17.4	5.6	60.4	22	50	35

Notes:

1) In order to improve dynamic performance, a feedforward capacitor (C_{FF}) can be considered to be in parallel with R_H.
2) Capacitor tolerance and bias voltage de-rating should be considered. The effective capacitance can vary by +20% and -80%. Please refer to the datasheet of the capacitor.
3) C_{OUT_NOM} is the minimum nominal capacitance value of C_{OUT} (output capacitance). C_{OUT_EFF} is the minimum effective capacitance value of C_{OUT}.

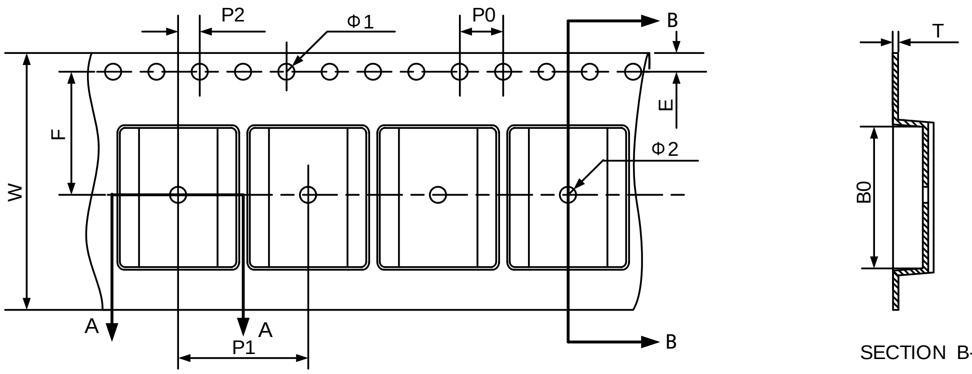
TAPE AND REEL INFORMATION

Reel UNIT: mm

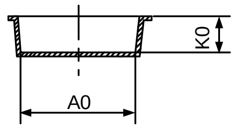


Package	Diameter Φ	Thickness W1	Width W2	W4
ESOP8	330±2	17.6±2	12.4±2	100±2

Carrier Tape UNIT: mm



SECTION B-B



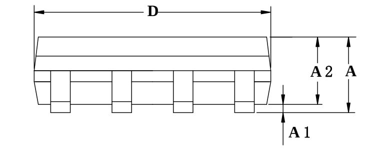
SECTION A-A

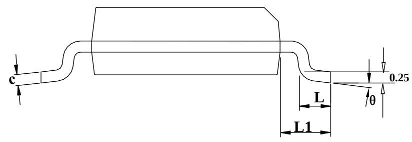
Note：
1) The carrier type is black, and colorless transparent.
2) Carrier camber is within 1mm in 100mm.
3) 10 pocket hole pitch cumulative tolerance:±0.20.
4) All dimensions are in mm.

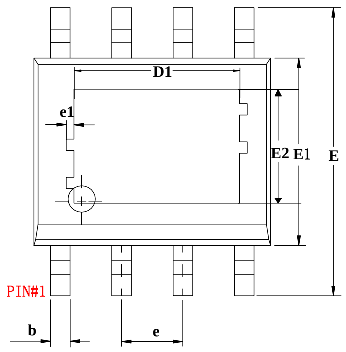
Package	Tape dimensions (mm)											
	P0	P2	P1	A0	B0	W	T	K0	Φ1	Φ2	E	F
ESOP8	4.0±0.1	2.0±0.1	8.0±0.1	6.40±0.3	5.35±0.3	12.0±0.3	0.25±0.2	2.00±0.2	1.50min	1.50min	1.75±0.1	5.50±0.10

PACKAGE OUTLINE

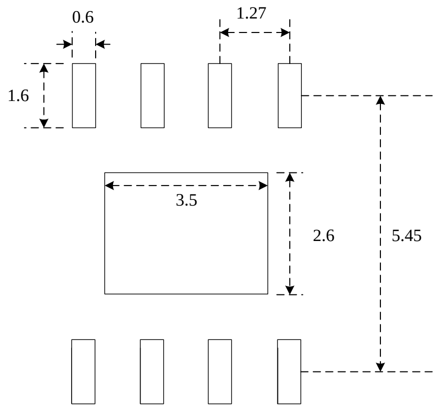
ESOP8 UNIT: mm







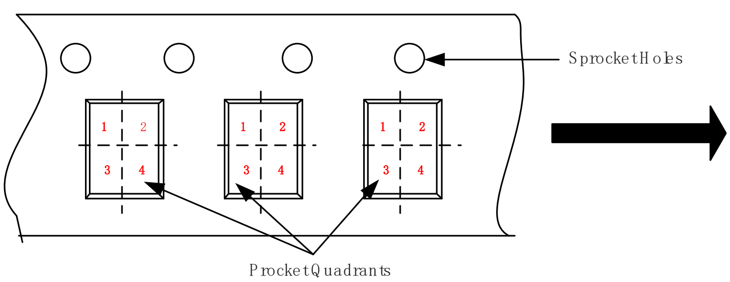
Symbol	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.65
A1	0.05	—	0.15
A2	1.30	1.40	1.50
b	0.39	—	0.47
c	0.20	—	0.24
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
L	0.50	0.60	0.80
L1	1.05REF		
θ	0°	—	8°



Recommend PCB Layout

Szie(mm) / L/F Szie (mil)	D1	E2	e1
90*90	2.09REF	2.09REF	0.16REF
95*130	3.10REF	2.21REF	0.10REF

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPAE



Package Type	Pin1 Quadrant
ESOP8	1

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