

60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

Features

- High Efficiency at Light Loads with Pulse Skipping
- 80-mΩ High-Side MOSFET
- 160-μA Operating Quiescent Current and 1-μA Shutdown Current
- 100-kHz to 2.5-MHz Adjustable Switching Frequency
- Integrated PLL to Synchronize with External Clock
- Adjustable UVLO Voltage and Hysteresis
- Under-voltage and Over-voltage Power Good Output
- Adjustable Soft-Start and Sequencing
- 0.8-V 1.5% Internal Voltage Reference
- 10-Pin DFN4X4-10 with Exposed Pad Package
- -40°C to 125°C Operation Temperature Range

Applications

- 12-V, 24-V, 48-V Industrial Power Application
- Telecom & Communication Equipment Power Applications

Description

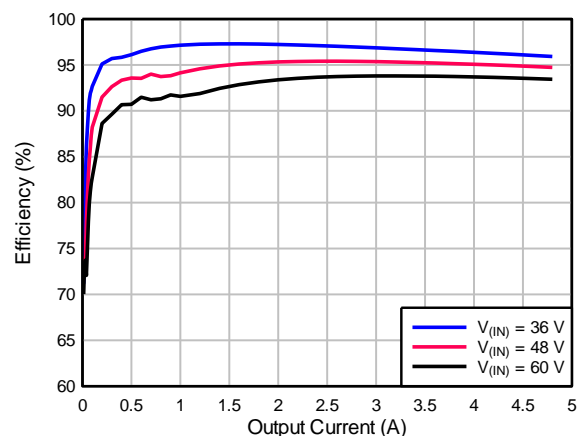
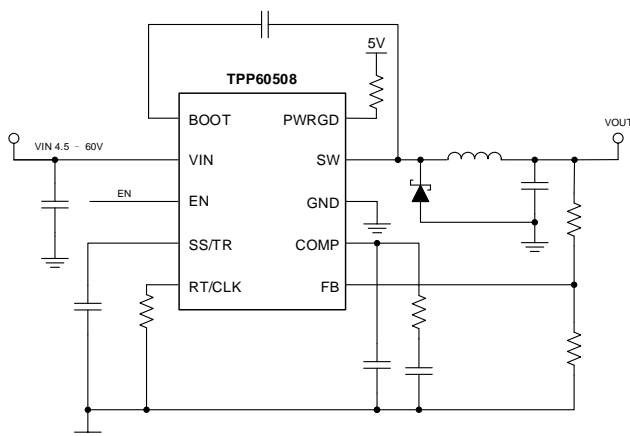
The TPP60508 is a 60-V, 5-A output, non-synchronous, step-down, switch-mode converter with integrated high-side power MOSFET.

The TPP60508 employs current-mode control supporting simple external compensation and flexible component selection. It also supports low quiescent current mode with pulse-skipping and ultra-low sleep current.

With integrated phase-locked loop, it can synchronize with external clock source with wide frequency selection, optimized for efficiency, physical dimensions, and electro-magnetic interference (EMI).

Protection and diagnostic features protect the device as well as the system power supply. By using open-drain powergood output, the user system is able to distinguish if the output supply is within target voltage range. The soft-start feature, which controls the output ramping, can be set independently with external resistors to soft-start or sequencing/tracking mode. Current-limit, frequency foldback and over temperature protection improves system-level robustness.

Typical Application Circuit



**60-V Input, 5-A, Non-Synchronous Step-Down
DC-DC Voltage Converter****Product Family Table**

Orderable Part Number	Package
TPP60508L1-DF9R-S	DFN4X4-10
TPP60508L1-DF9R	DFN4X4-10

Table of Contents

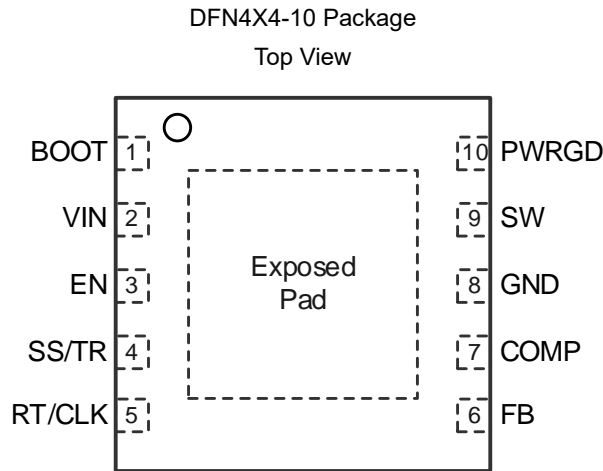
Features	1
Applications	1
Description	1
Typical Application Circuit	1
Product Family Table	2
Revision History	4
Pin Configuration and Functions	5
Pin Functions.....	5
Specifications	6
Absolute Maximum Ratings.....	6
ESD, Electrostatic Discharge Protection	6
Recommended Operating Conditions	7
Thermal Information	7
Electrical Characteristics	8
Typical Performance Characteristics.....	10
Detailed Description	16
Overview.....	16
Functional Block Diagram	16
Feature Description	16
Application and Implementation	20
Application Information.....	20
Typical Application	20
Tape and Reel Information	21
Package Outline Dimensions	22
DFN4X4-10.....	22
Order Information	23

**60-V Input, 5-A, Non-Synchronous Step-Down
DC-DC Voltage Converter****Revision History**

Date	Revision	Notes
2022-2-10	Rev.A.0	Initial Release Version

60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

Pin Configuration and Functions



Pin Functions

Pin		I/O	Description
No.	Name		
1	BOOT	I	Bootstrap capacitor between BOOT and SW, recommend to use a 0.1- μ F ceramic capacitor with 10-V or higher voltage rating.
2	VIN	O	Supply voltage with 4.5-V to 60-V operating range
3	EN	O	Device enable pin with internal pull-up current source. Threshold can be increased via external resistors.
4	SS/TR	I	Soft-start and tracking input. When using soft-start mode, an external capacitor connected to this pin sets output ramping time; When using track/sequence mode, the voltage on this pin overrides internal voltage reference thus sets the output voltage.
5	RT/CLK	-	Frequency selection and external clock input. When using it as frequency setting mode, an external connected resistor sets switching frequency; When using it as clock synchronization input, the input is a high impedance clock input for internal PLL.
6	FB	I	Feedback input, connected to internal inverting input of gm error amplifier
7	COMP	I/O	Error amplifier output and input to the PWM comparator, Connect frequency compensation network to this pin
8	GND	G	Device ground pin
9	SW	O	Switching output
10	PWRGD	O	Open-drain power good output
11	Exposed Pad	G	Device exposed pad, must be connected to GND with heat sink area for thermal dissipation.

60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

Specifications

Absolute Maximum Ratings

Parameter		Min	Max	Unit
VIN	Supply Voltage	-0.3	65	V
SW	Switching Node Voltage	-0.3	VIN + 0.3	V
	Switching Node Voltage, SW 5-ns Transient	-7	VIN + 0.3	V
	Switching Node Voltage, SW 10-ns Transient	-2	VIN + 0.3	V
BOOT – SW	Bootstrap Voltage	-0.3	6.5	V
FB	Feedback Voltage	-0.3	3	V
COMP	Compensation Voltage	-0.3	3	V
EN	Enable Input Voltage	-0.3	8.4	V
SS/TR	Soft start / Tracking Input Voltage	-0.3	3	V
RT/CLK	Switching frequency setting / PLL Input	-0.3	3	V
TJ	Operating Junction Temperature Range	-40	150	°C
TA	Ambient Temperature Range	-40	125	°C
TSTG	Storage Temperature Range	-65	150	°C
TL	Lead Temperature (Soldering, 10 sec)		260	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

ESD, Electrostatic Discharge Protection

Symbol	Parameter	Condition	Minimum Level	Unit
HBM	Human Body Model ESD	ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
CDM	Charged Device Model ESD	ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

Recommended Operating Conditions

Parameter		Min	Max	Unit
VIN	Supply Voltage	- 0.3	65	V
SW	Switching Node Voltage	- 0.3	VIN + 0.3	V
	Switching Node Voltage, SW 5-ns Transient	- 7	VIN + 0.3	V
	Switching Node Voltage, SW 10-ns Transient	- 2	VIN + 0.3	V
BOOT – SW	Bootstrap Voltage	- 0.3	6.5	V
FB	Feedback Voltage	- 0.3	3	V
COMP	Compensation Voltage	- 0.3	3	V
EN	Enable Input Voltage	- 0.3	8.4	V
SS/TR	Soft start / Tracking Input Voltage	- 0.3	3	V
RT/CLK	Switching frequency setting / PLL Input	- 0.3	3	V
T _J	Operating Junction Temperature Range	- 40	150	°C
T _A	Ambient Temperature Range	- 40	125	°C
T _{STG}	Storage Temperature Range	- 65	150	°C
T _L	Lead Temperature (Soldering, 10 sec)		260	°C

Thermal Information

Package Type	θ_{JA}	θ_{JC}	Unit
DFN4X4-10	TBD	TBD	°C/W

(1) This data was taken with the JEDEC low effective thermal conductivity test board.

(2) This data was taken with the JEDEC standard multilayer test boards.

60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

Electrical Characteristics

All test condition is $V_{IN} = 4.5\text{ V to }60\text{ V}$, $T_J = -40^\circ\text{C to }150^\circ\text{C}$, unless otherwise noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply						
V_{IN}	Operating Voltage Range		4.5		60	V
$V_{(UVLO)}$	Internal undervoltage lockout threshold	Rising threshold	4.1	4.3	4.48	V
$V_{(UVLO,hys)}$				325		mV
I_Q	Quiescent supply current	$EN = 5\text{ V}$, $T_A = 25^\circ\text{C}$, $V_{(FB)} = 0.9\text{ V}$		152	200	μA
I_{QSD}	Shut down supply current	$EN = 0\text{ V}$, $T_A = 25^\circ\text{C}$		10.8	18	μA
VFB Voltage						
V_{FB}	V_{FB} Threshold Voltage		0.788	0.8	0.812	mV
MOSFET						
$HS_{RDS(on)}$	HS Switching On-Resistance	$V_{IN} = 12\text{ V}$, $BOOT - SW = 5\text{ V}$		80	185	m Ω
Current Limit						
I_{Limit}	Current Limit	Full voltage and temperature range, Open-Loop	6.3	7.9	10	A
		Full temperature range, $V_{IN} = 12\text{ V}$, Open-Loop	6.6	7.9	8.9	A
		$T_A = 25^\circ\text{C}$, $V_{IN} = 12\text{ V}$, Open-Loop	6.7	7.9	8.7	A
Error Amplifier						
$I_{(FB)}$	Input current			50		nA
g_m	Error amplifier transconductance	$-2\ \mu\text{A} < I_{COMP} < 2\ \mu\text{A}$, $V_{COMP} = 1\text{ V}$		350		μMhos
g_m	Error amplifier transconductance during soft-start	$-2\ \mu\text{A} < I_{COMP} < 2\ \mu\text{A}$, $V_{COMP} = 1\text{ V}$, $V_{FB} = 0.4\text{ V}$		77		μMhos
A_{DC}	Error amplifier gain	$V_{(FB)} = 0.8\text{ V}$		10000		V/V
$f_{(GBW),min}$	Minimal unity gain bandwidth			2500		kHz
$I_{(COMP)}$	Error amplifier output current capability	$V_{(COMP)} = 1\text{ V}$, 100-mV overdrive		± 31		μA
$g_{COMP-SW}$	COMP to SW current transconductance			17		A/V
Thermal Shutdown						
T_{SD}	Thermal shut down temperature			165		$^\circ\text{C}$
T_{HYS}	Thermal hysteresis			15		$^\circ\text{C}$
Power Good (PWRGD)						
$V_{th(UV-falling)}$	Output undervoltage falling threshold			90		%
$V_{th(UV-rising)}$	Output undervoltage rising threshold			93		%
$V_{th(OV-falling)}$	Output overvoltage falling threshold			108		%

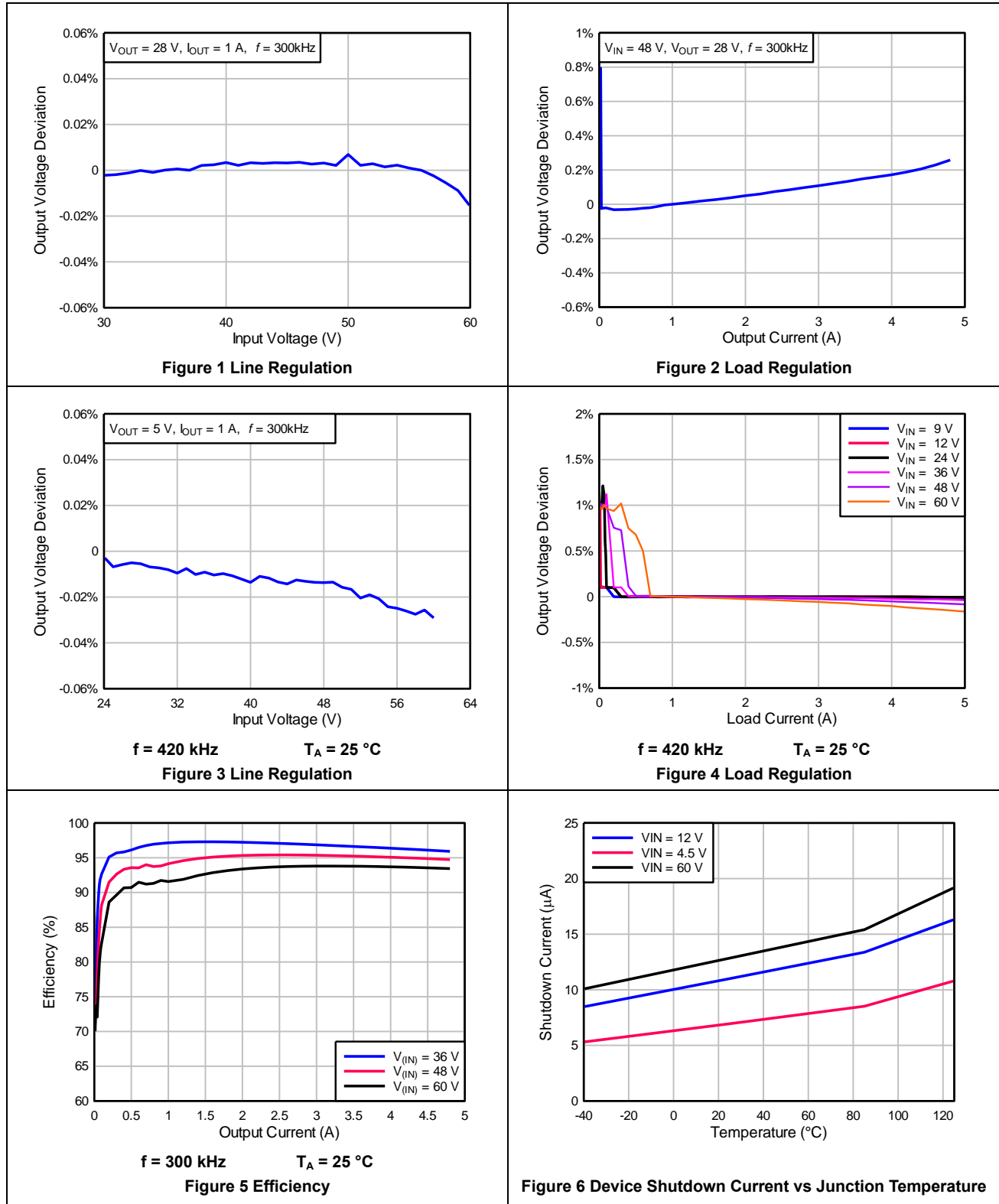
60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
$V_{th(OV-rising)}$	Output overvoltage rising threshold			106		%
$V_{th(hys)}$	Output hysteresis	FB falling		2.5		%
$I_{lkg(PWRGD)}$	PWRGD leakage current	$V_{(PWRGD)} = 5.5\text{ V}$, $T_A = 25\text{ }^\circ\text{C}$		10		nA
$R_{dson(PWRGD)}$	PWRGD on-resistance	$I_{(PWRGD)} = 3\text{ mA}$, $V_{FB} < 0.79\text{ V}$		6.5		Ω
$V_{(minVIN,PWRGD)}$	Minimal VIN for defined output	$V_{(PWRGD)} < 1.5\text{ V}$, $I_{(PWRGD)} = 1.5\text{ mA}$		2	2.5	V
Soft Start and Tracking (SS/TR)						
$I_{(SS/TR)}$	Soft-start charging current	$V_{(SS/TR)} = 0.4\text{ V}$		1.7		μA
$\Delta V_{(SS/TR)}$	SS/TR to FB matching error	$V_{(SS/TR)} = 0.4\text{ V}$		42		mV
$I_{(SS/TR),disch}$	Max SS/TR discharge current	$V_{(FB)} = 0\text{ V}$, $V_{(SS/TR)} = 0.4\text{ V}$		1		mA
$V_{(SS/TR),disch}$	SS/TR discharge voltage	$V_{(FB)} = 0\text{ V}$		54		mV
$V_{(SS/TR),th}$	SS/TR to reference cross-over threshold			1.2		V
LOGIC						
V_{EN}	EN threshold voltage		1.1	1.2	1.3	V
I_{EN}	EN threshold + 50 mV			-4.6		μA
	EN threshold -50 mV		-0.58	-1.2	-1.8	μA
$I_{EN,hys}$	EN threshold hysteresis		-2.2	-3.4	-4.5	μA
$V_{th(RT/CLK),rising}$	RT/CLK rising threshold			1.55	2	V
$V_{th(RT/CLK),falling}$	RT/CLK falling threshold		0.5	1.2		V
Timing Characteristics						
t_{OCP}	Over current protection delay			60		ns
$t_{d,EN}$	Enable to COMP delay			540		μs
$t_{CLK,min}$	Minimal CLK input pulse width			15		ns
$t_{d,CLK}$	RT/CLK falling edge to SW rising edge delay	$f_{sw} = 500\text{ kHz}$		55		ns
f_{sw}	Switching frequency	$R_T = 200\text{ k}\Omega$	450	500	550	kHz
	Switching frequency using RT mode		100		2500	kHz
	Switching frequency using CLK mode		160		2300	kHz
t_{PLL}	PLL lock in time	$f_{sw} = 500\text{ kHz}$		78		μs

60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

Typical Performance Characteristics

All test condition: $V_{OUT} = 5\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.



60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

Typical Performance Characteristics (Continued)

All test condition: $V_{IN} = 48\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.

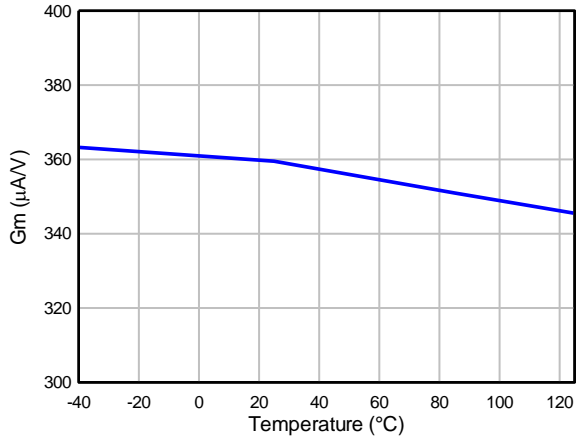


Figure 7. Error Amplifier Transconductance vs Junction Temperature

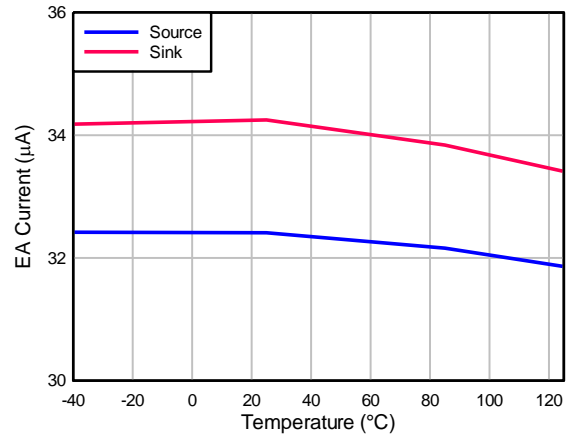
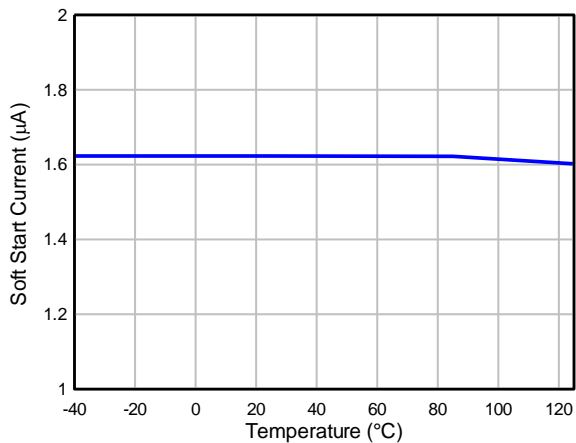


Figure 8 Error Amplifier Sink Current vs Junction Temperature



$V_{IN} = 48\text{ V}$ $T_A = 25^\circ\text{C}$

Figure 9 Soft Start Charge Current vs Junction Temperature

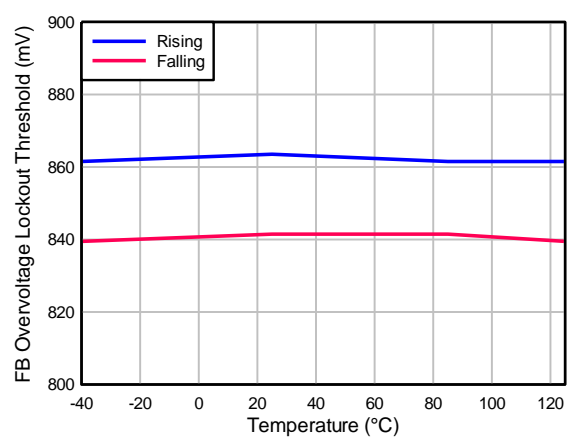


Figure 10 FB Overvoltage Lockout Threshold vs Temperature

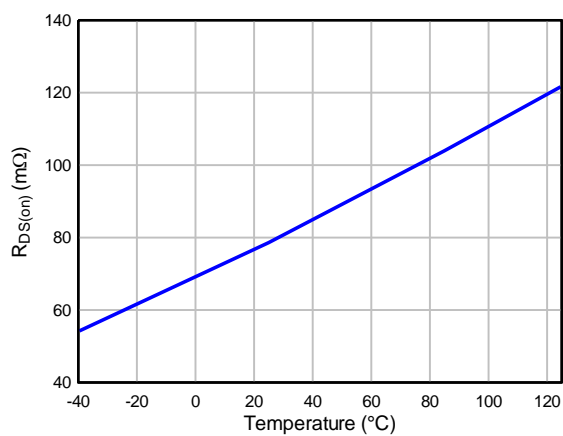


Figure 11 Power Transistor On-Resistance vs Temperature

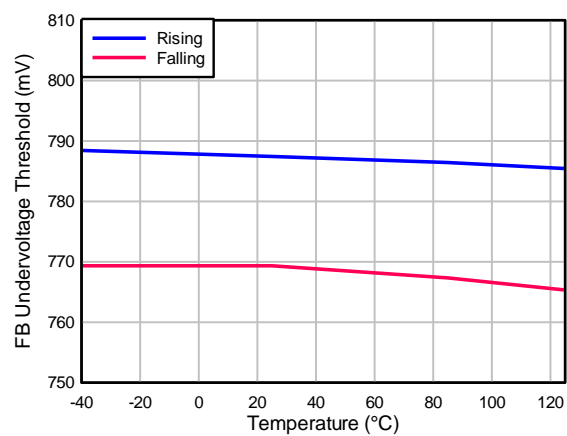
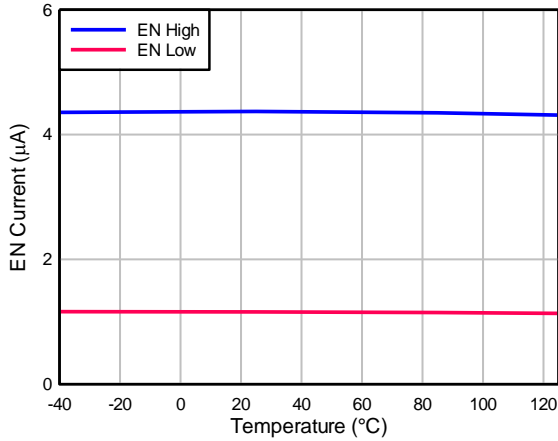


Figure 12 FB Undervoltage Lockout Threshold vs Temperature

60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

Typical Performance Characteristics (Continued)

All test condition: $V_{OUT} = 48\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.



$T_A = 25^\circ\text{C}$

Figure 13 EN Current vs Junction Temperature

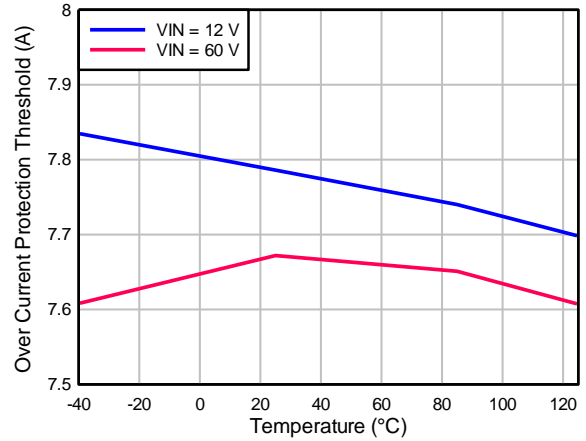
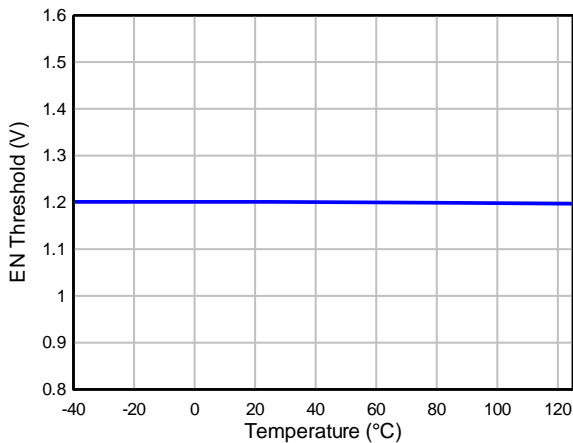
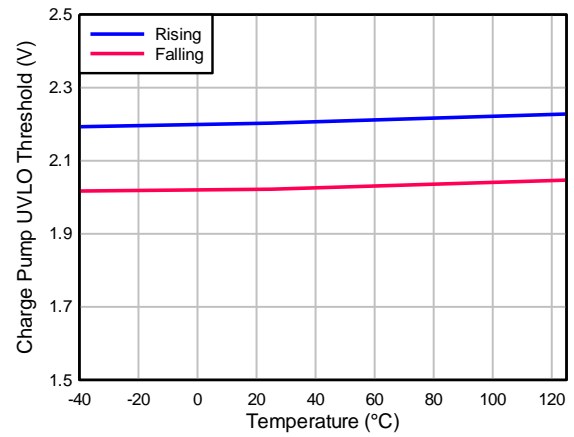


Figure 14 Over Current Protection Threshold vs Junction Temperature



$V_{IN} = 12\text{ V}$

Figure 15 EN Threshold vs Junction Temperature



$V_{IN} = 12\text{ V}$

Figure 16 BOOT-SW UVLO vs Junction Temperature

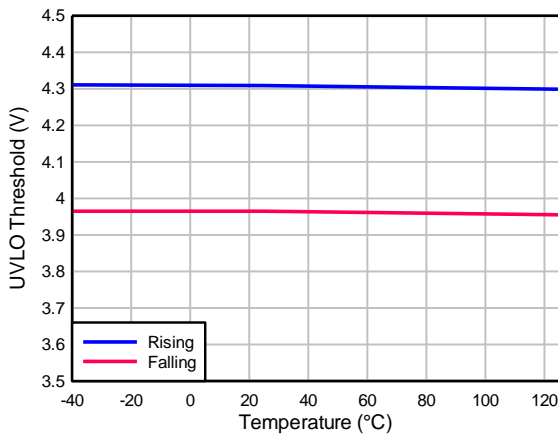


Figure 17 UVLO Threshold vs Junction Temperature

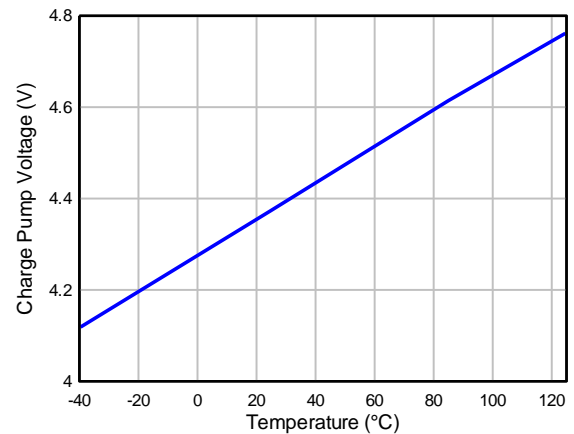
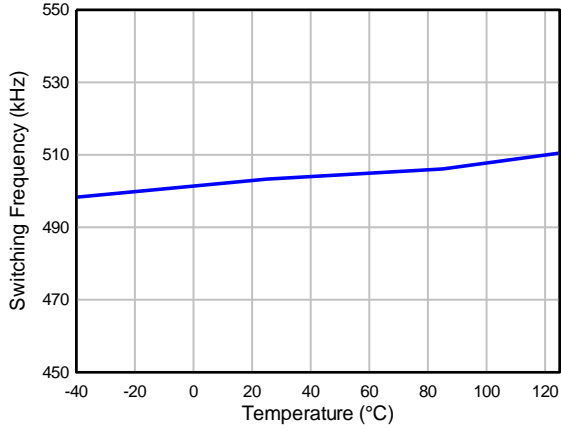


Figure 18 BOOT-SW Voltage vs Temperature

60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

Typical Performance Characteristics (Continued)

All test condition: $V_{IN} = 48\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.



$R_{RT} = 200\text{ k}\Omega$

Figure 19 Switching Frequency vs Junction Temperature

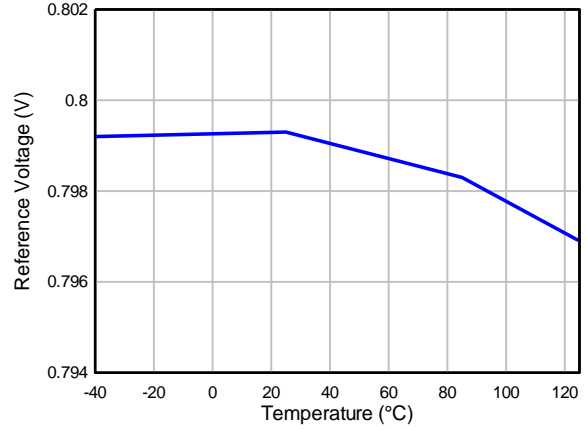


Figure 20 Reference Voltage vs Junction Temperature

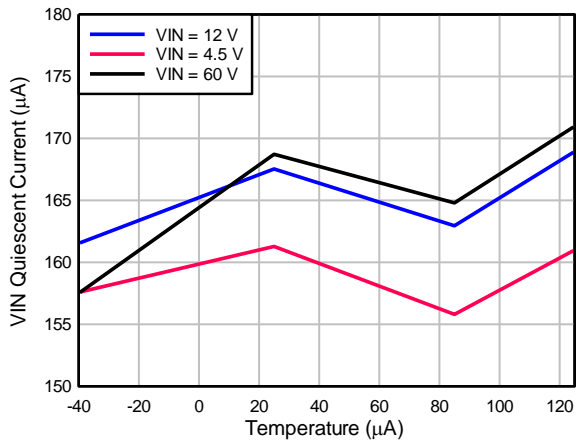


Figure 21 Device Quiescent Current vs Junction Temperature

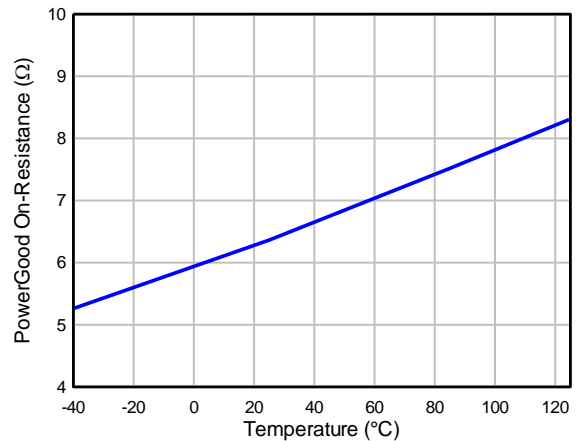
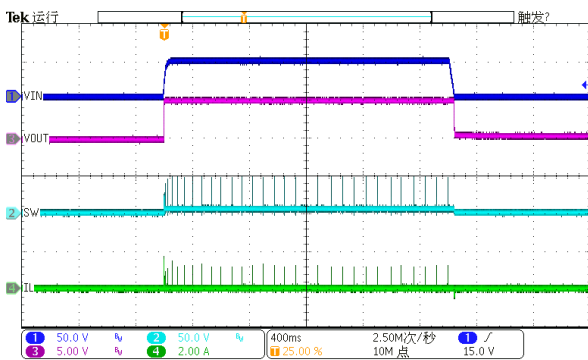
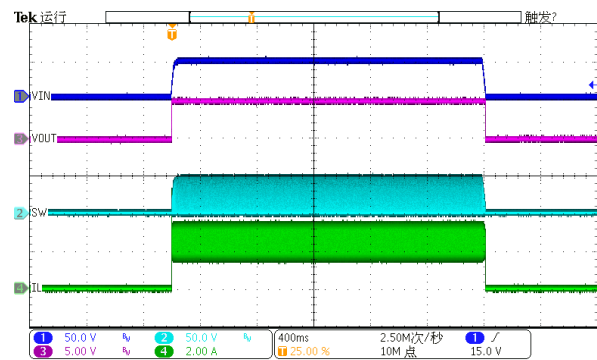


Figure 22 PWRGD On-resistance vs Junction Temperature



$V_{IN} = 48\text{ V}$ $I_{OUT} = 0\text{ A}$ $T_A = 25^\circ\text{C}$
Figure 23 Power Cycle Without Load Current

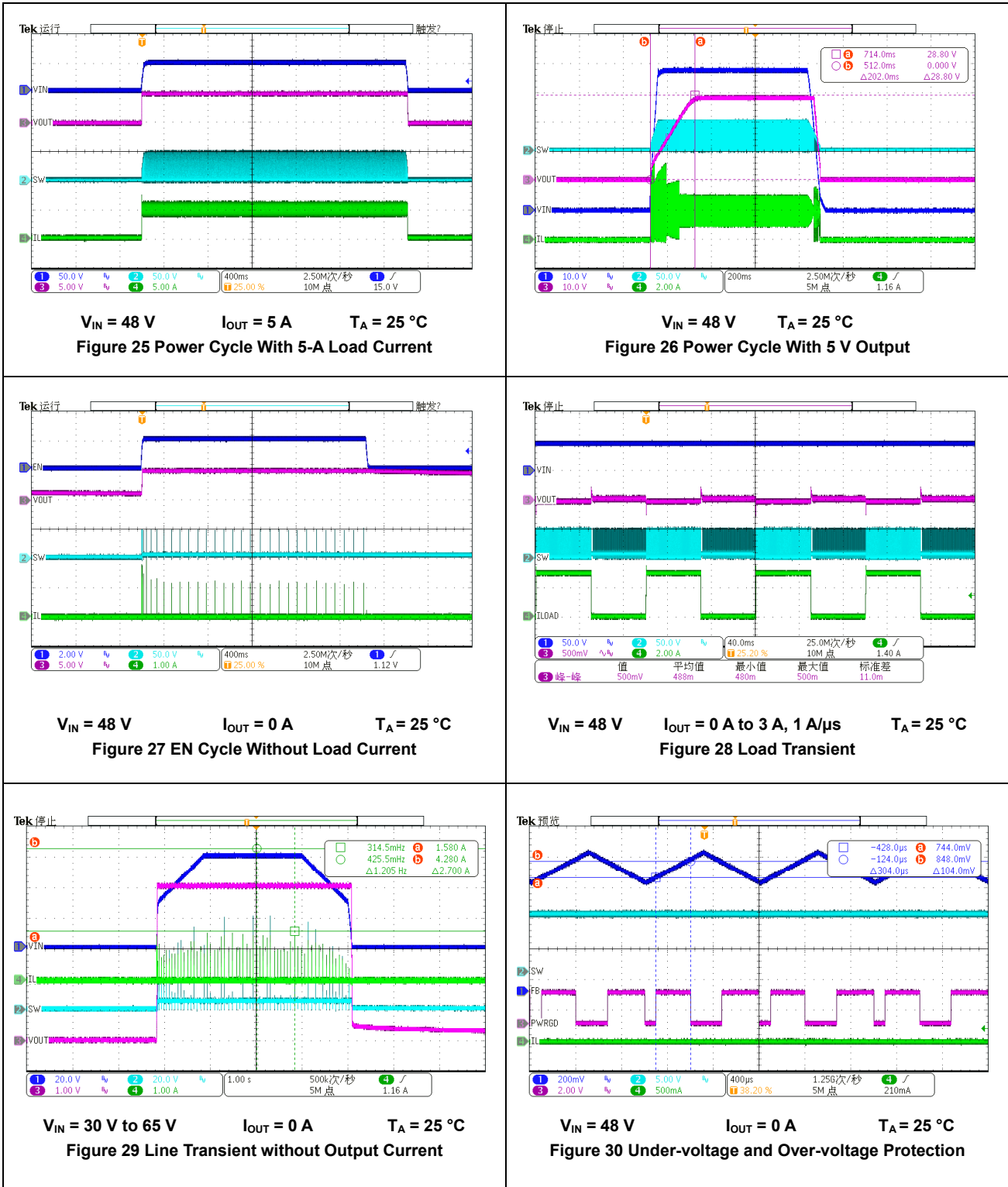


$V_{IN} = 48\text{ V}$ $I_{OUT} = 2.5\text{ A}$ $T_A = 25^\circ\text{C}$
Figure 24 Power Cycle With 2.5-A Load Current

60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

Typical Performance Characteristics (Continued)

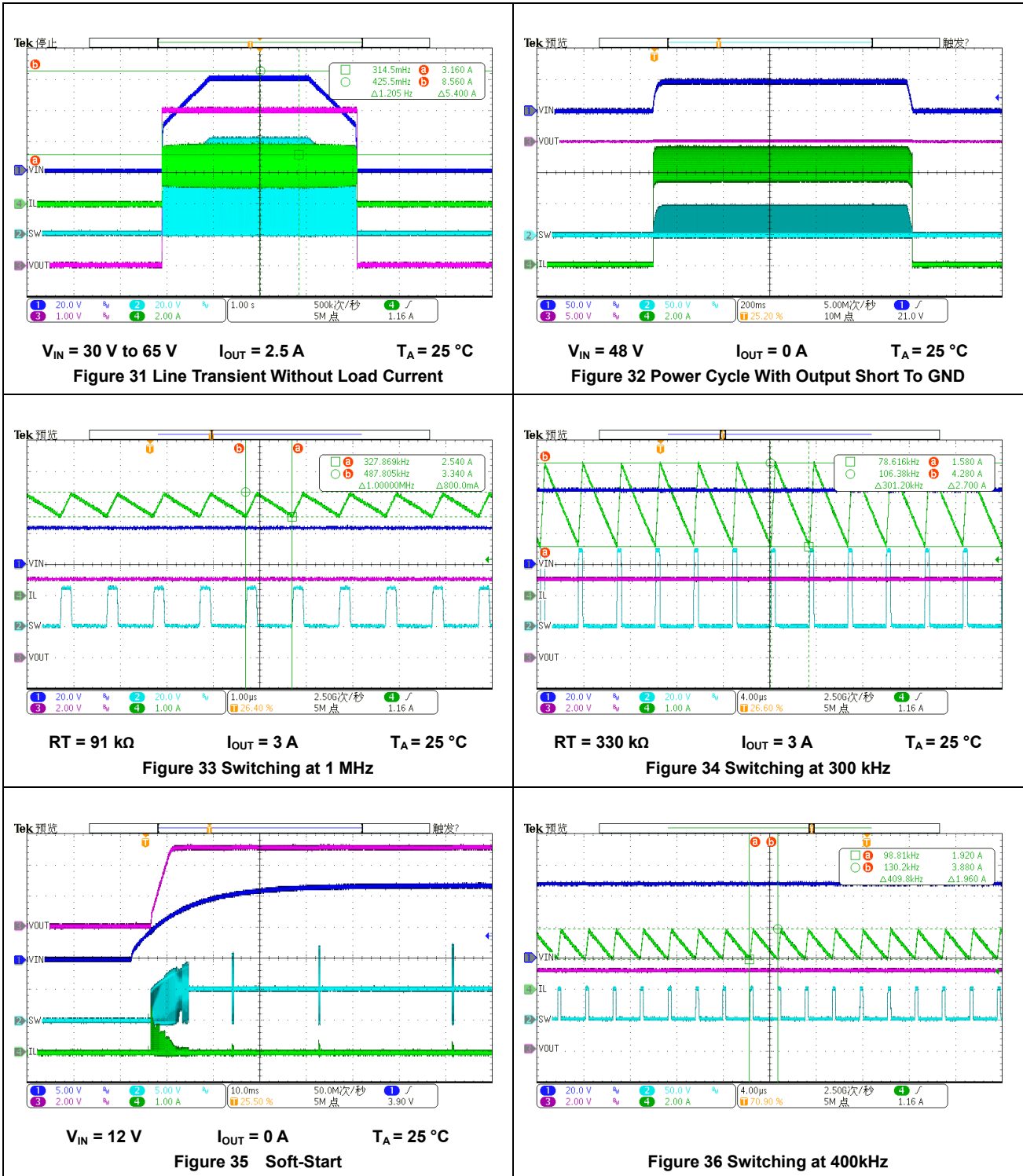
All test condition: $V_{IN} = 48\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.



60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

Typical Performance Characteristics (Continued)

All test condition: $V_{IN} = 48\text{ V}$, $T_A = +25^\circ\text{C}$, unless otherwise noted.



60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

Detailed Description

Overview

The TPP60508 is a 60-V, 5-A output, non-synchronous, step-down, switch-mode converter with integrated high-side power MOSFET.

The TPP60508 employs current mode control supporting simple external compensation and flexible component selection. It also supports low quiescent current mode with pulse-skipping and ultra-low sleep current.

With integrated phase-locked loop, it can synchronize with external clock source with wide frequency selection, optimized for efficiency, physical dimensions and electro-magnetic interference (EMI).

Protection and diagnostics features protect the device as well as the system power supply. By using open-drain powergood output, system is able to distinguish if the output supply is within the target voltage range. Soft-start features, which controls the output ramping, can be set independently by external resistor or to sequencing/tracking mode. Current-limit, frequency foldback and over temperature protection improves system-level robustness.

Functional Block Diagram

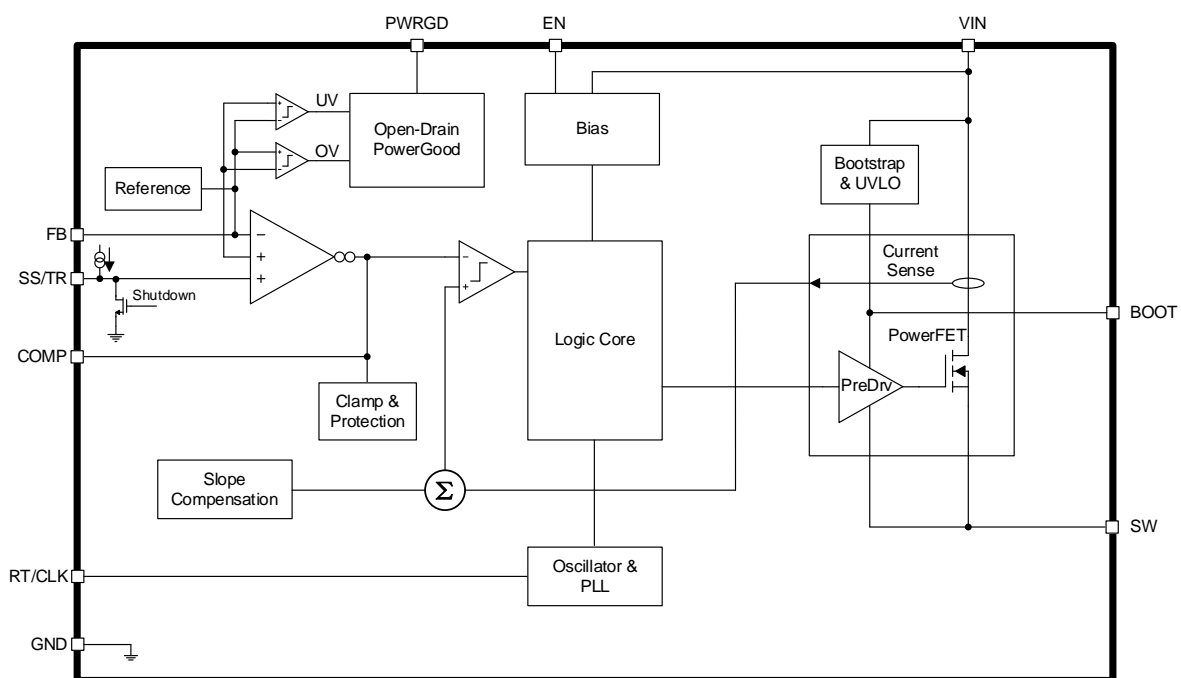


Figure 37 Functional Block Diagram

Feature Description

Fixed Frequency Peak Current Mode Control

The TPP60508 uses peak current mode control with adjustable switching frequency. The feedback voltage is sensed through FB pin to compare with internal voltage reference by an error amplifier. The output of the error amplifier is compared by PWM comparator with internal voltage ramp and controls high-side power switch. Internal oscillator controls the frequency of switching high-side MOSFET.

60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

The high-side switching current is sensed internally as part of the voltage ramp. The internal voltage ramp compensates control loop from sub-harmonic oscillations when duty-cycles are greater than 50%. Once the PWM comparator detects peak switching current reaches the threshold level set by COMP voltage, the high-side MOSFET is switched off. The COMP pin is also clamped for current limiting and pulse-skipping mode.

The transconductance error amplifier converts the error voltage between FB pin voltage and internal voltage, whichever lower of the soft-start voltage or internal voltage reference V_{FB} , to current with transconductance g_m of 350 μ Mhos during normal operation conditions. During soft-start operation, transconductance is reduced to ensure smooth soft-start. It is recommended to connect compensation network between COMP and GND pin to ensure stability across all working ranges. The details are discussed in the application chapter.

Setting Output Voltage

The precision internal voltage reference produces a 0.8-V voltage reference with $\pm 1.5\%$ tolerance across operating temperature and voltage ranges. The resistor divider from output voltage to FB pin sets the output voltage.

$$R_H = R_L \times \left(\frac{V_{OUT} - V_{FB}}{V_{FB}} \right) \quad (1)$$

Pulse-Skipping Light-Load Operation

The TPP60508 enters into pulse-skipping operation when peak switching current is below internal threshold. In the pulse-skipping mode, the device clamps COMP at 0.6 V and stops switching high-side MOSFET. As the output voltage falls and differential input voltage increase, the error amplifier output increases. When the COMP voltage rises above the pulse skipping threshold, the device resumes switching high-side MOSFET.

The current threshold is equivalent to the current of a nominal COMP voltage at 1V. As the device uses peak switching current for pulse-skipping threshold, the threshold is also dependent on the output inductance.

Soft-Start with Pre-Biased Capability

The device uses SS/TR node to implement a programmable soft-start feature by controlling ramping up reference voltage. The reference voltage will be the lower of internal reference voltage and SS/TR voltage. The timing of soft-start is programmable via external capacitor connected to SS/TR node.

An internal constant-current source of 1.7 μ A charges up the external SS/TR capacitor to an internally clamped 2.7V. The timing can be calculated as below equation, measured from 10% to 90%.

$$T_{SS} = \frac{V_{REF} \times C_{SS} \times (90\% - 10\%)}{I_{SS}} \quad (2)$$

To ensure proper start-up, the device will discharge SS/TR voltage upon powering up if SS/TR voltage is above 54 mV. During any case the device stops switching, such as undervoltage lockout (UVLO), EN pulled low or over temperature protection, the device will discharge SS/TR below 54mV before switching.

The device also supports using SS/TR input for tracking as well as power supply sequencing. Sequencing needs to be carefully designed to ensure the system is able to recover from any fault.

RT/CLK

The device supports wide switching frequency from 100kHz to 2500kHz. The frequency is programmable via

60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

resistor connected between RT/CLK and GND. The switching frequency will affect solution size, efficiency, and minimal duty cycle. It is suggested that all factors taken care of when selecting switching frequency. The resistor can be calculated via equation

$$f = \frac{k}{R_{RT}} \quad (3)$$

The device switching clock supports external clock sources for synchronization. Once a square wave is applied at the RT/CLK pin, the rising edge of SW synchronizes to the falling edge of RT/CLK. It is also suggested to connect a frequency set resistor to RT/CLK pin in case external clock source is not available.

The first rising edge of RT/CLK sets the device from free-running frequency mode to synchronization mode. The internal 0.5V voltage source is removed and the RT/CLK is set to high impedance mode. It takes 78μs to lock on external clock frequency; When external clock source stops, the device will switch back to free running frequency mode with frequency set by external resistor. During the transition, the device frequency will stay at 70kHz and then switch to the free-running frequency.

The device will foldback frequency by 1, 2, 4 and 8 depending on the FB voltage. This is to ensure that during normal start-up and fault conditions, the device is able to increase its period and off time. This is helpful when output is short-circuit to GND, the longer off time allows inductor current to decay.

Protection

Undervoltage Lockout (UVLO)

The device has undervoltage lockout feature with default rising threshold of 4.3 V. It can be adjusted by using EN pin with external resistors. A weak current source of 1.2 μA pulls up the EN pin to internal voltage rail. Another 3.4-μA hysteresis current source provides hysteresis voltage between rising and falling threshold. The resistor values can be calculated via below equations.

$V_{SYS_UVLO_H}$ is the desired system level undervoltage protection rising threshold voltage, $V_{SYS_UVLO_L}$ is the desired system level undervoltage protection falling threshold voltage. R_{UVLOH} and R_{UVLOL} are depicted in Figure 38.

$$R_{UVLOH} = \frac{V_{SYS_UVLO_H} - V_{SYS_UVLO_L}}{I_{EN_hys}} \quad (4)$$

$$R_{UVLOL} = \frac{V_{EN}}{\frac{V_{SYS_UVLO_H} - V_{EN}}{R_{UVLOH}} + I_{EN}} \quad (5)$$

60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

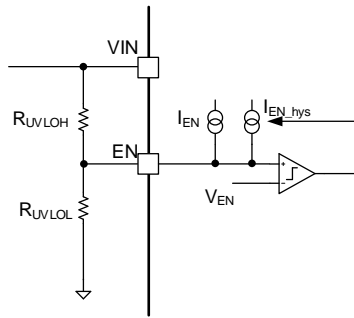


Figure 38 Using EN as UVLO threshold adjustment

Over Current Protection

The device employs peak current mode control by controlling the peak current of internal high-side power transistor. The high side transistor current is converted to a voltage signal and compared to COMP pin. When the peak switching current is above the threshold set by COMP voltage, the device turns off high-side power transistor.

When the device is in over current scenario, the output voltage is pulled low and device will increase switching current threshold until it reaches the internal current limit threshold. Once the switching current is above the threshold, the device will turn off the transistor as current limit. Delay needs to be taken in to account that may cause the peak inductor current slightly higher than open-loop current limit.

Once the over current load is removed, the device will resume normal operation in the following cycle.

Power Good

The device uses an open-drain output PWRGD to signal if the output voltage is operating within the boundaries. If the FB voltage is within the 93% and 106% of internal reference voltage, the PWRGD pull-down will be disabled and pulled up by externally resistor. The external pull up voltage source is recommended to be less than 5.5V with a 1kΩ resistor. If FB voltage is lower than 90% or greater than 108% of internal reference voltage, the PWRGD will be pulled low.

If UVLO, over temperature protection or EN going low, the PWRGD will also be pulled low. When supply voltage is below 2V, the PWRGD may not be at any defined state.

Over Voltage Protection

The device stops high-side FET switching when it detects FB voltage above the over voltage protection (OVP) rising threshold (108% of internal reference voltage). When the voltage falls below the falling threshold (106% of internal reference voltage), it resumes switching high-side FET. With the OVP feature, the device is able to minimize voltage overshoot during load transient with low output capacitance.

Over Temperature Shutdown

When the devices sense the junction temperature above the internal rising threshold of 175°C, the device stops high-side FET switching. Once the device junction temperature falls below falling threshold 165°C, the device restart the device with power up sequence.

The device will discharge the SS/TR to GND as part of power up sequence. Care must be taken that the SS/TR is able to be pulled low to avoid deadlock scenario that may prevent the device re-start.

60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

Application and Implementation

NOTE

Information in the following applications sections is not part of the 3PEAK's component specification and 3PEAK does not warrant its accuracy or completeness. 3PEAK's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

Application Information

The TPP60508 is a non-synchronous 60-V 5-A step-down regulator with integrated high-side FET. The device is capable to support a wide range of voltage rails including 12-V, 24-V and 48-V. It is widely used in communication, industrial and automotive applications.

Typical Application

Figure 39 shows the typical application schematic of the TPP60508.

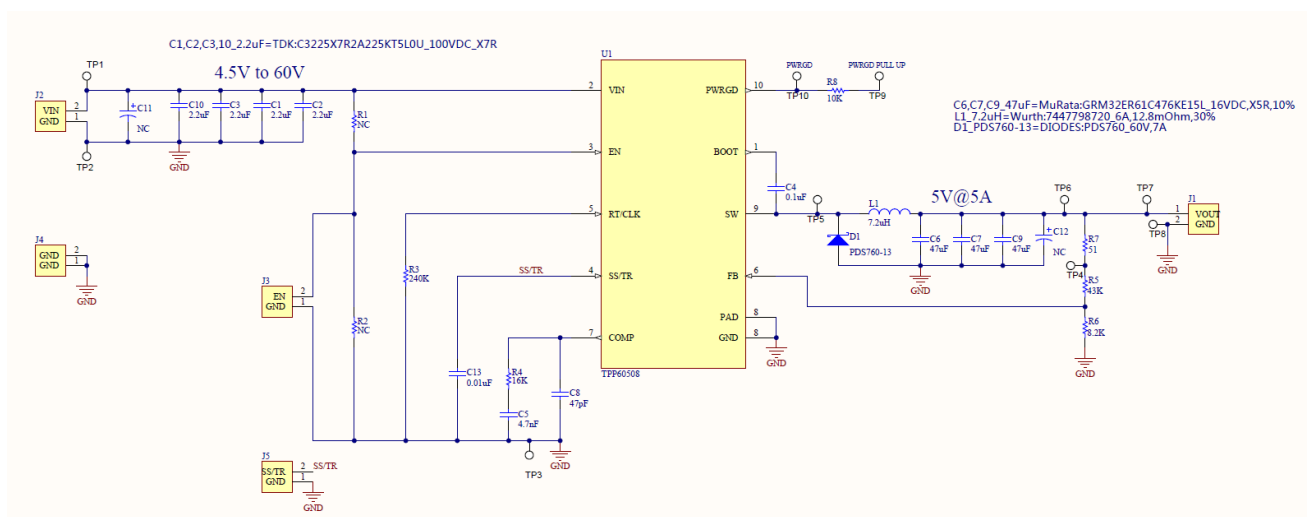
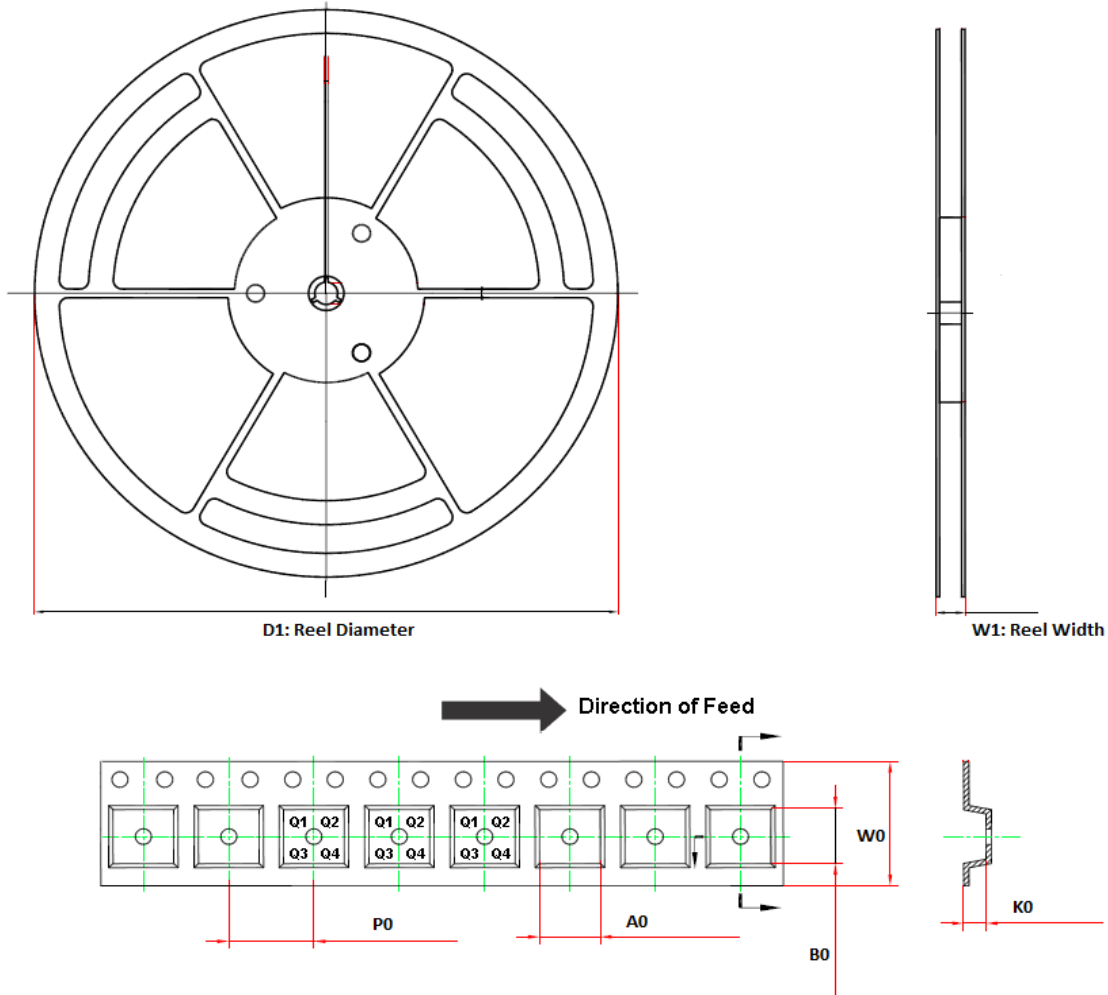


Figure 39 TPP60508 Typical Application Circuit

Tape and Reel Information

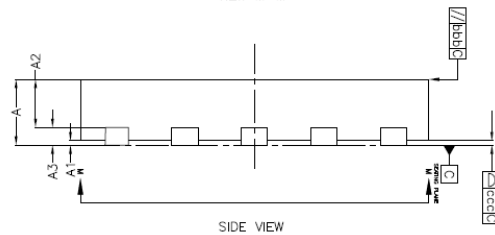
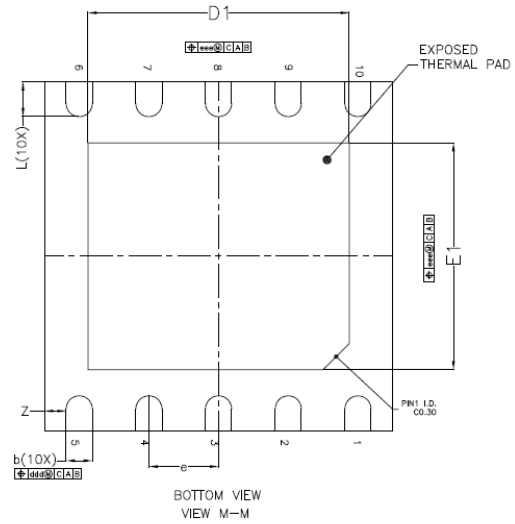
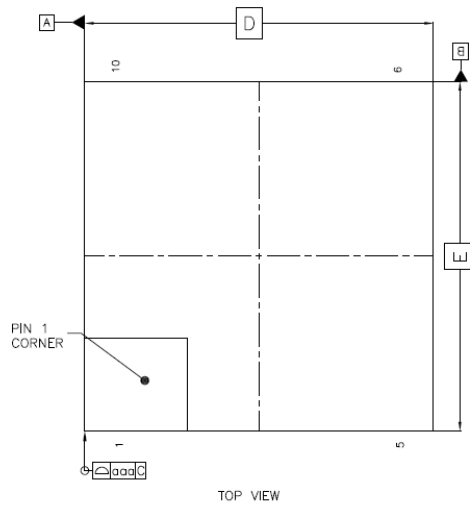


Order Number	Package	D1 (mm)	W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	W0 (mm)	Pin1 Quadrant
TPP60508L1-DF9R-S	DFN4X4-10	330	17.6	4.2	4.2	1.1	8.0	12	Q1
TPP60508L1-DF9R	DFN4X4-10	330	17.6	4.2	4.2	1.1	8.0	12	Q1

60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

Package Outline Dimensions

DFN4X4-10



DESCRIPTION	SYMBOL	MILLIMETER			
		MIN	NEW	MAX	
TOTAL THICKNESS	A	0.75	0.75	0.80	
STAND OFF	A1	0.00	0.035	0.05	
MOLD THICKNESS	A2	0.50	0.55	0.60	
L/F THICKNESS	A3	0.203 REF			
BODY SIZE	X	D	3.90	4.00	4.10
	Y	E	3.90	4.00	4.10
LEAD PITCH	e	0.80 BSC			
LEAD TO PKG SPACE	Z	0.25 BSC			
LEAD WIDTH	b	0.25	0.30	0.35	
LEAD LENGTH	L	0.35	0.40	0.45	
EP SIZE	D1	2.95	3.00	3.05	
	E1	2.55	2.60	2.65	
Tolerance of form and position					
PACKAGE EDGE TOLERANCE	aaa	0.1			
MOLD FLATNESS	bbb	0.1			
COPLANARITY	ccc	0.08			
LEAD OFFSET	ddd	0.1			
EXPOSED PAD OFFSET	eee	0.1			

NOTES
1.0 COPLANARITY APPLIES TO LEADS, CORNER LEADS AND DIE ATTACH PAD.

60-V Input, 5-A, Non-Synchronous Step-Down DC-DC Voltage Converter

Order Information

Order Number	Operating Temperature Range	Package	Marking Information	MSL	Transport Media, Quantity	Eco Plan
TPP60508L1-DF9R-S	-40°C to 125°C	DFN4X4-10	P658	Level 1	Tape & Reel, 3000	Green
TPP60508L1-DF9R	-40°C to 125°C	DFN4X4-10	P658	Level 1	Tape & Reel, 3000	Green

Green: 3PEAK defines "Green" to mean RoHS compatible and free of halogen substances.

 **3PEAK and the 3PEAK logo are registered trademarks of 3PEAK INCORPORATED. All other trademarks are the property of their respective owners.**

